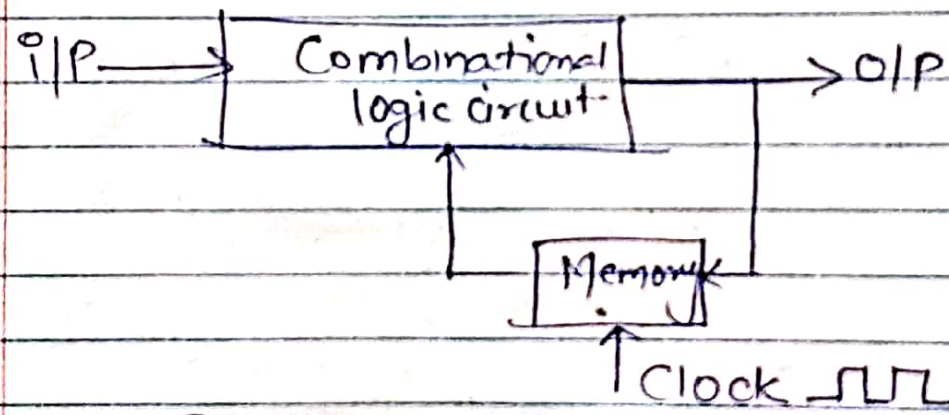
Flipflops

Combinational circuit:-

- o/p depends only on level present at i/p terminals
- Don't use memory
- Clock signal is not used.
- e.g. full adder, full subtractor, multiplexer

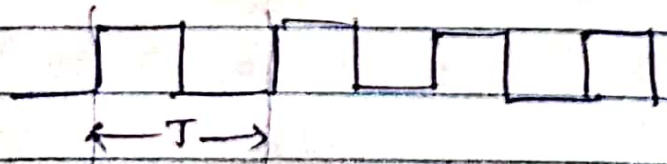
Sequential circuit

- o/p depends upon present i/p, previous o/p,
- for previous o/p memory is required.
- clock signal is present.



- eg. flipflops, Register, counter

Clock signal

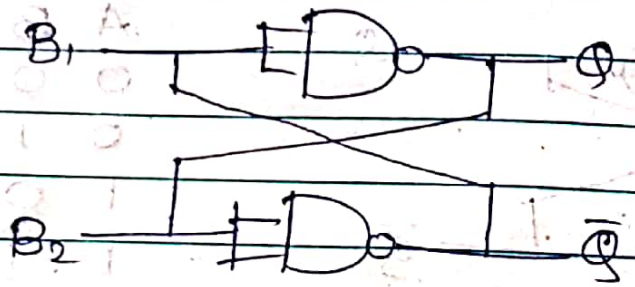


It is a timing signal applied as an i/p signal with duty cycle.

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Flip Flop

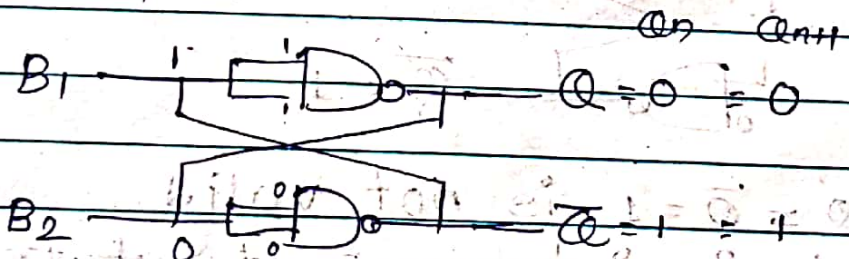
- It is a basic memory elements.
- It is a 1 bit memory cell.
- It is design using two NAND/NOR gates & has two stable states 0 & 1.
- o/p of gate 1 is connected to i/p of gate 2 & o/p of gate 2 is connected to i/p of gate 1.



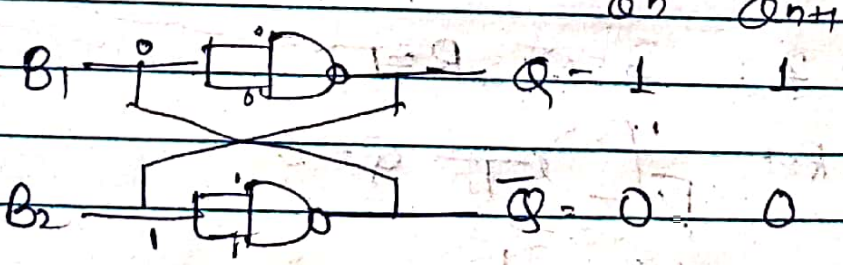


A	B	$\overline{AB}$
0	0	1
0	1	1
1	0	1
1	1	0

Case 1 ⇒ Q = 0



Case 2 ⇒ Q = 1



① They will never be equal.
$Q = \bar{Q} \neq 0$ ... $Q = \bar{Q} \neq 1$

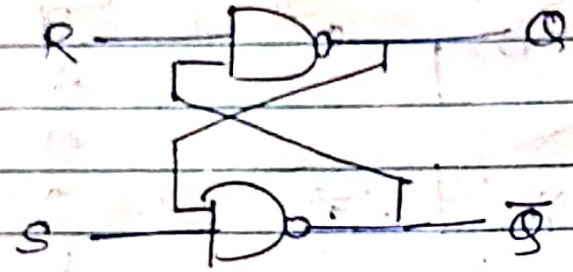
② Q = 1, $\bar{Q}$ = 0 ⟶ Set state
Q = 0, $\bar{Q}$ = 1 ⟶ Reset state

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Flip flop

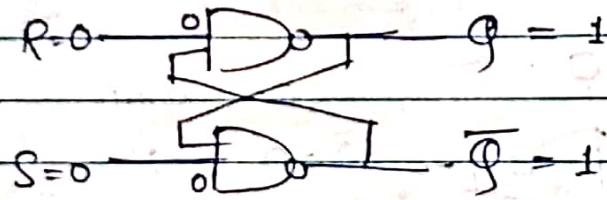
1. SR latch
2. SR flip flop
3. D flip-flop
4. T flip flop
5. JK flip-flop

① SR Latch using NAND gates



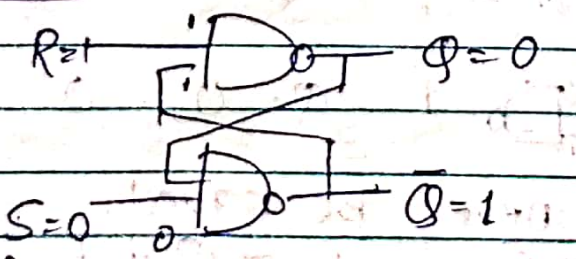
A	B	$\overline{AB}$
0	0	1
0	1	1
1	0	1
1	1	0

Case 1: S=0 & R=0



$Q = \bar{Q} = 1$ is not valid which is indeterminate state & called as "RACE condition".

Case 2: S=0 R=1

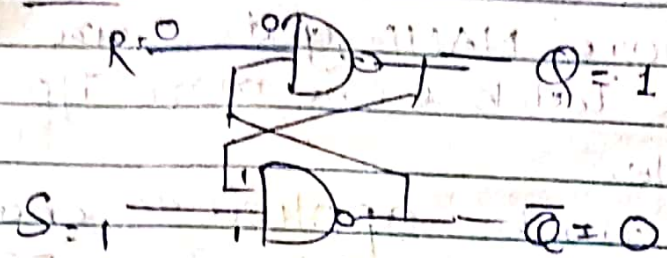


if S=0 & R=1 then we get $Q = 0$ & $\bar{Q} = 1$

This is called 'RESET condition'.

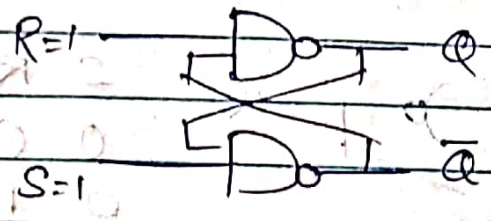
SHOT ON MI A2
MI DUAL CAMERA
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Case 3 : S = 1 ; R = 0



When S = 1 & R = 0 then
we get Q = 1 & $\bar{Q}$ = 0
This is set condition

Case 4 S = 1 R = 1



$Q = \overline{R\bar{Q}}$ $\quad\quad$ $\bar{Q} = \overline{SQ}$

$= \bar{R} + \bar{\bar{Q}}$ $\quad\quad$ $= \bar{S} + \bar{Q}$

$= 0 + Q$ $\quad\quad$ $= 0 + \bar{Q}$

$= Q$ $\quad\quad$ $= \bar{Q}$

When S = 1 & R = 1
we get $Q = Q$ $\bar{Q} = \bar{Q}$
This is "No change condition"

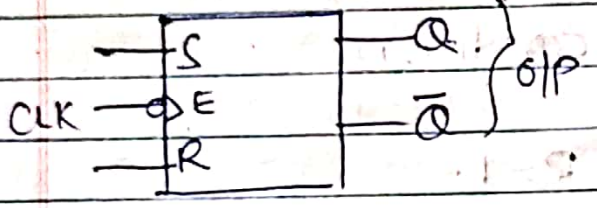
Truth Table of SR Latch

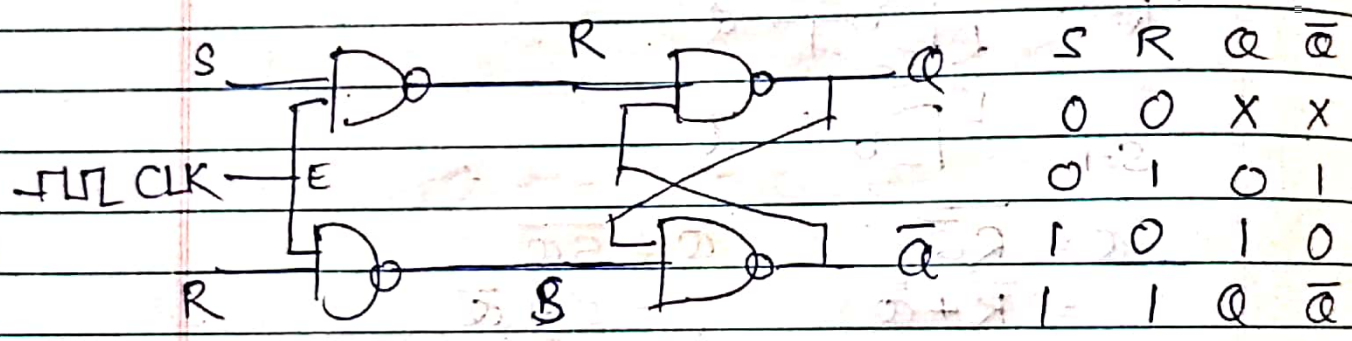
S	R	Q_n	$\bar{Q}_n$	
0	0	X	X	RACE
0	1	0	1	RESET
1	0	1	0	SET
1	1	Q	$\bar{Q}$	No change

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Gated Latch - SRFF

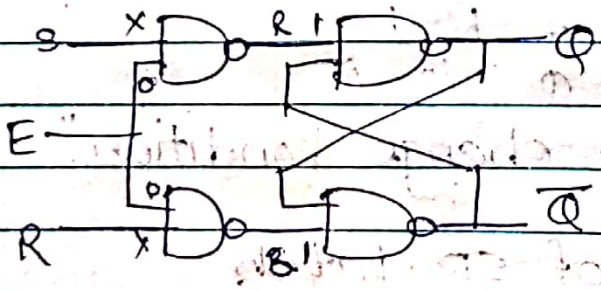
- In this 2 more NAND gates are added to basic SR latch & one more i/p called Enable
- Clock signal can be applied to enable(E)
- FF are called "level triggered FF" / gated latch / clocked FF.





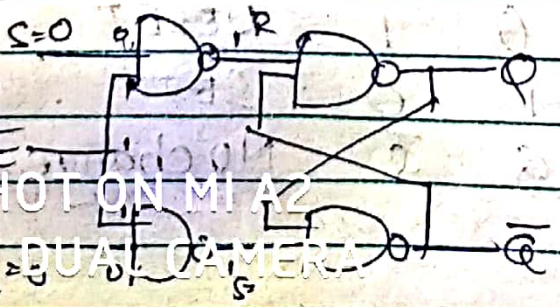
S	R	Q	$\bar{Q}$
0	0	X	X
0	1	0	1
1	0	1	0
1	1	Q	$\bar{Q}$

Case 1: E=0 S=X R=X



No change

Case 2: E=1 S=0 R=0

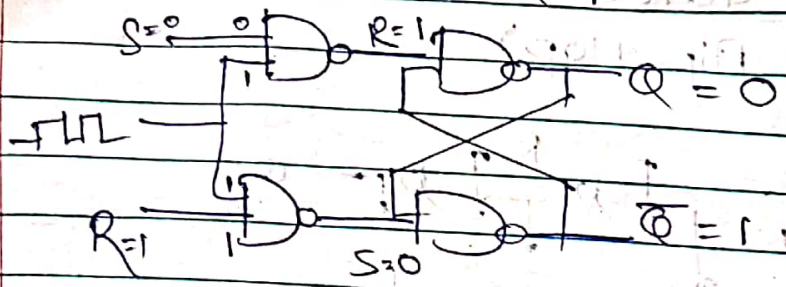


No change

SHOT ON MI A2
MI DUAL CAMERA

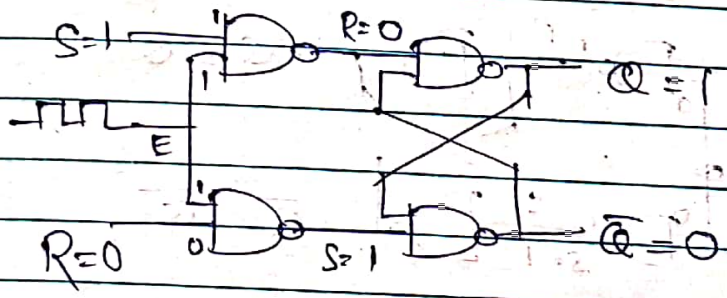
Scanned with CamScanner

case 3: E=1 S=0 R=1



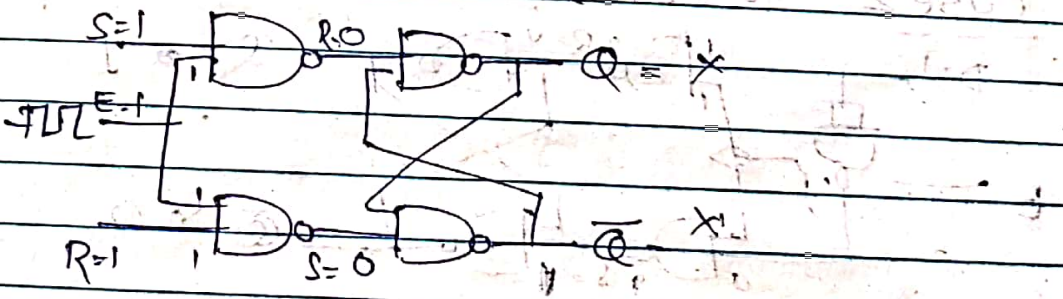
Reset condition

Case 4: E=1 S=1 R=0



Set condition

Case 5: E=1 S=1 R=1



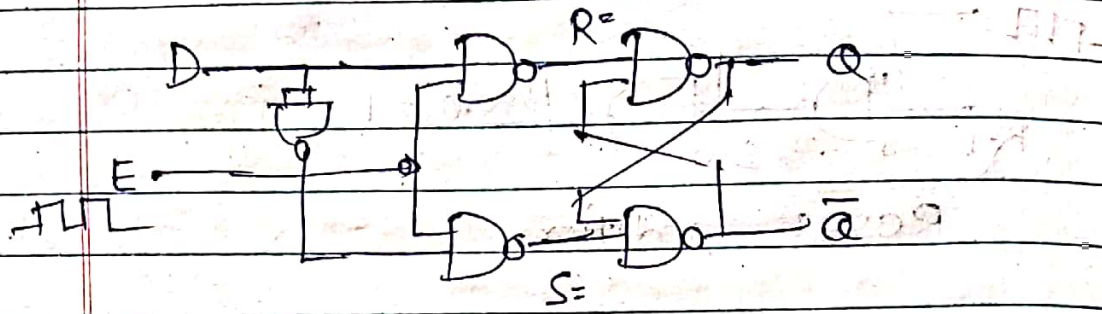
RACE condition

Truth Table SR FF

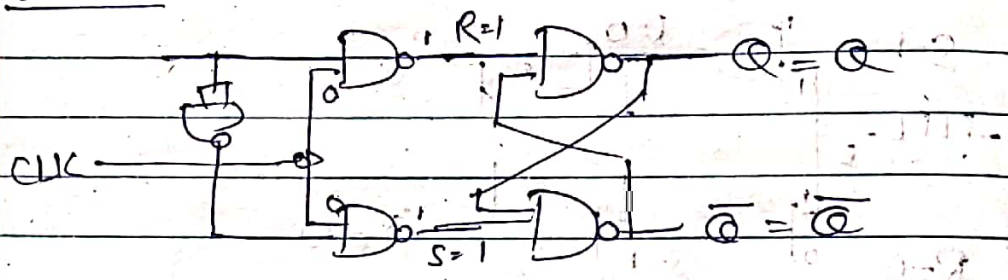
E	S	R	Q	$\bar{Q}$	
0	X	X	Q	$\bar{Q}$	No change
1	0	0	Q	$\bar{Q}$	No change
1	0	1	0	1	RESET
1	1	0	1	0	SET
1	1	1	X	X	RACE

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DFF (Gated D Latch)
(Data flip flop)

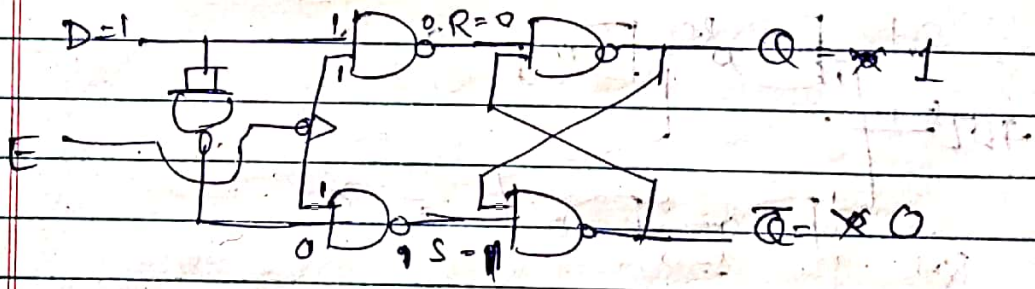


Case 1 E=0 D=X



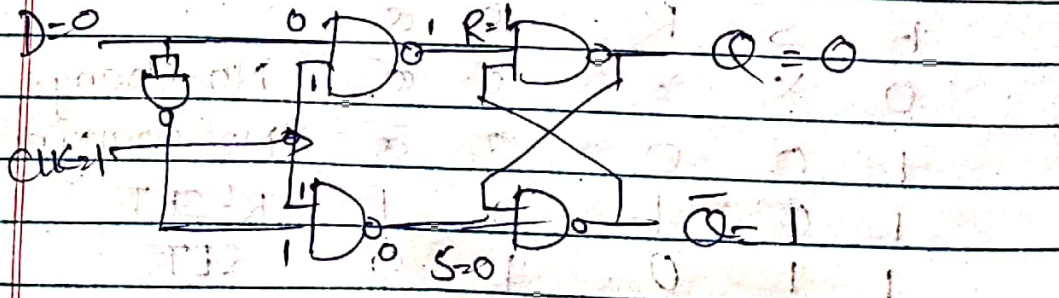
No change

Case 2 E=1 D=1



~~RACE~~ Set condition

Case 3 E=1 D=0



RESET cond^n

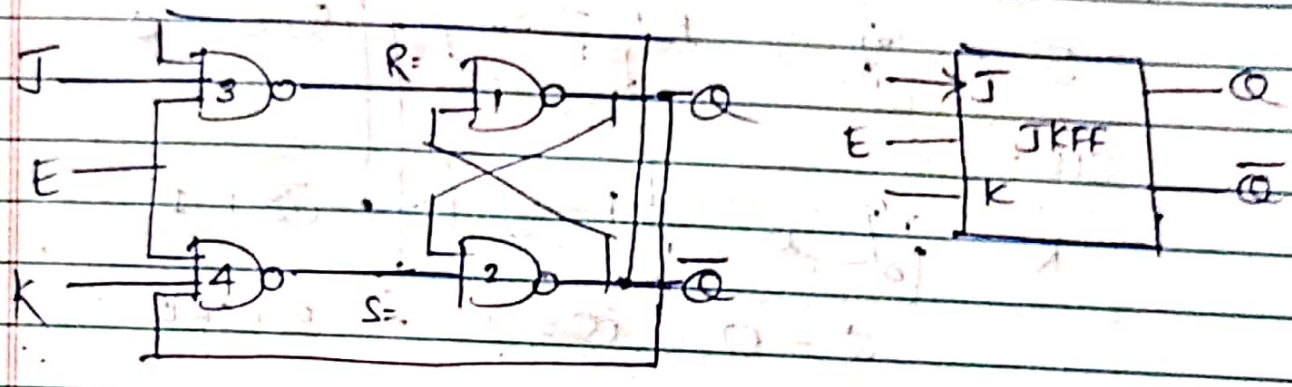
Scanned with CamScanner

Truth Table

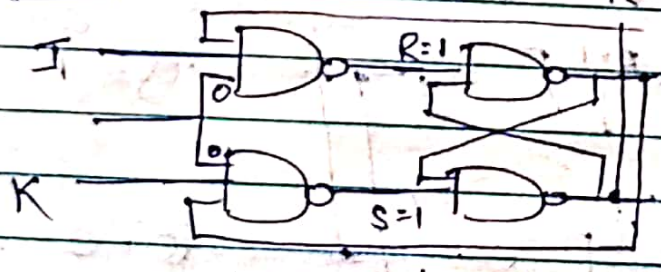
E	D	Q	$\bar{Q}$	
0	X	Q	$\bar{Q}$	No change
1	0	0	1	Reset cond^n
1	1	1	0	Set cond^n

JKFF (JK-flip-flop)

(Jack kilby : Invented IC in 1958

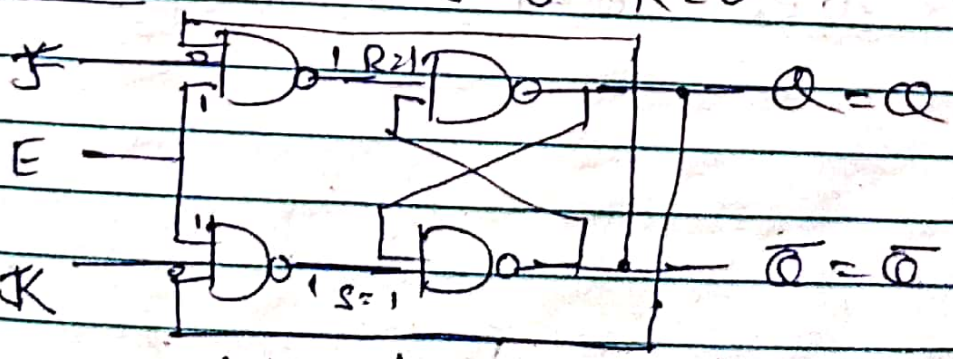


case 1 E=0 J=X K=X



No change

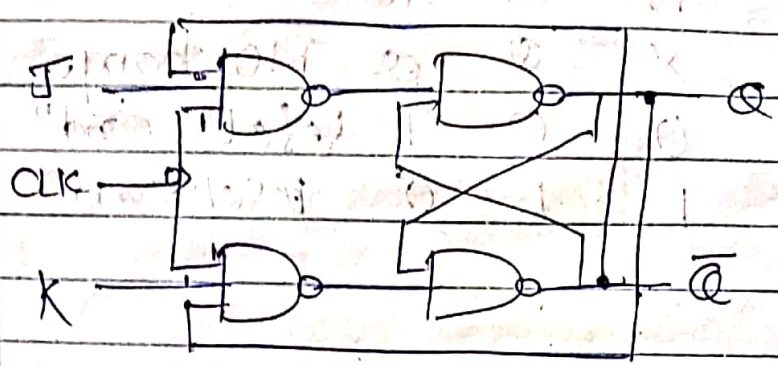
case 2 E=1 J=0 K=0



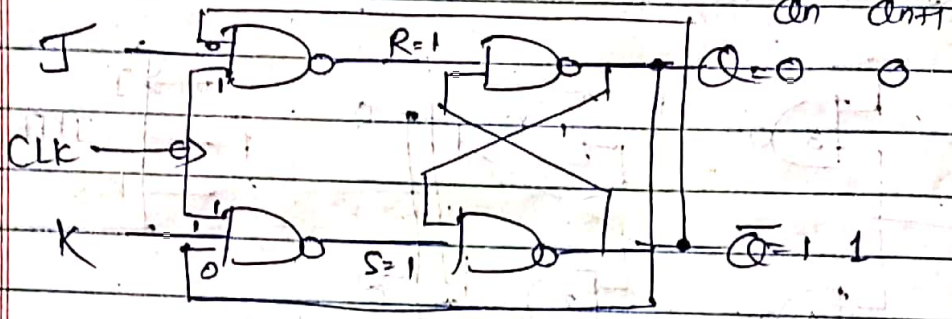
No change

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Case 3 E=1 J=0 K=1

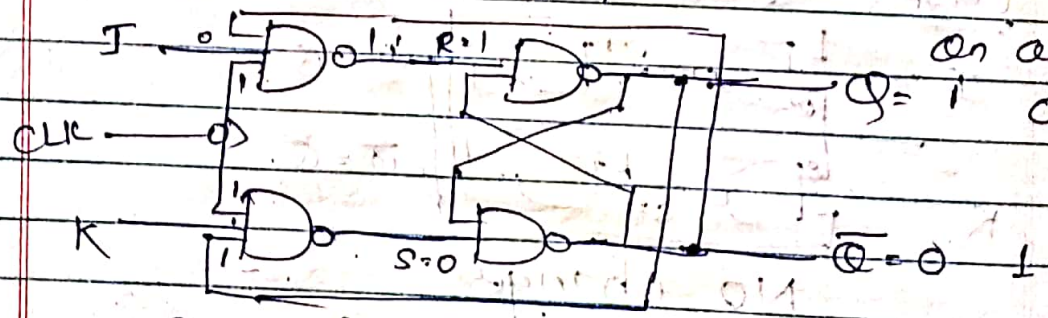


① Q=0 J=0 K=1



Q=0 $\bar{Q}$=1 → Reset

② Q=1 J=0 K=1

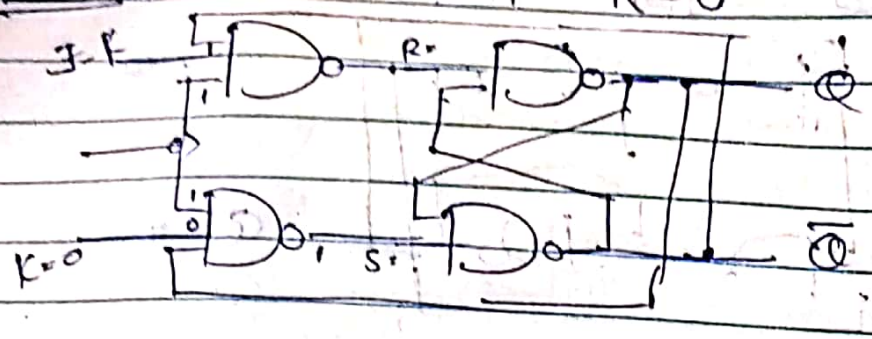


Q=1 $\bar{Q}$=0 S=0 R=1

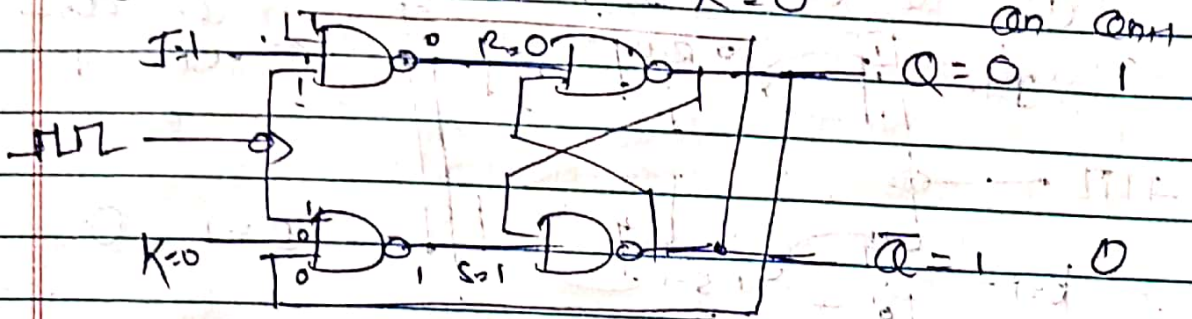
Q=0 $\bar{Q}$=1 → Reset

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Case 4 E=1 J=1 K=0



① Q=0 J=1 K=0



Q_n Q_{n+1}

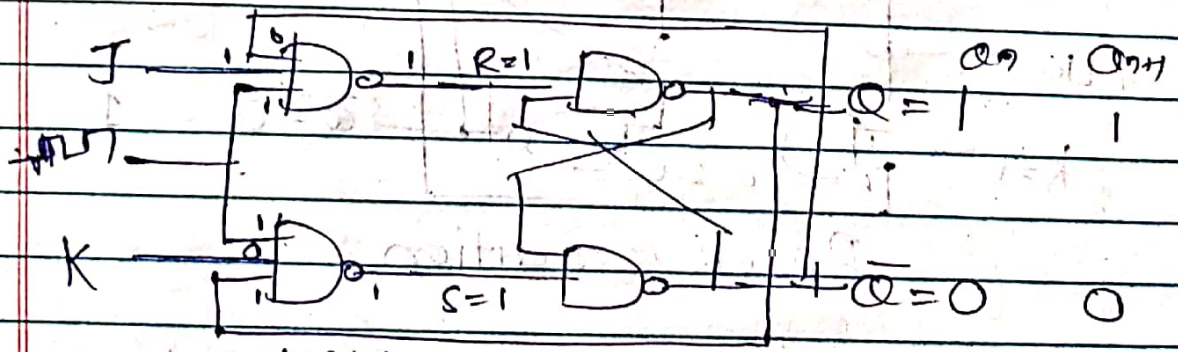
0 1

1 0

When S=1 R=0

Set condition

② Q=1 J=1 K=0



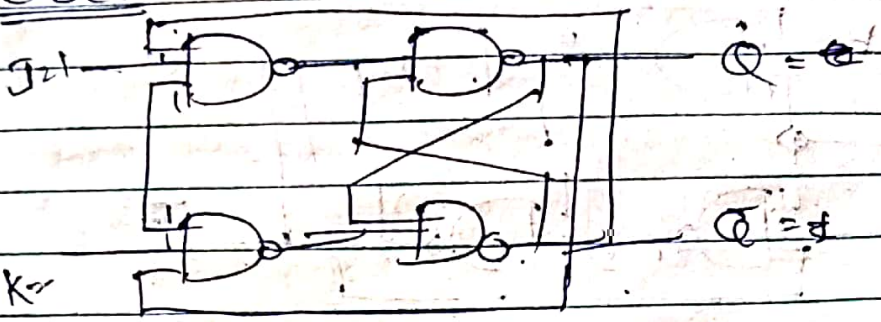
Q_n Q_{n+1}

1 1

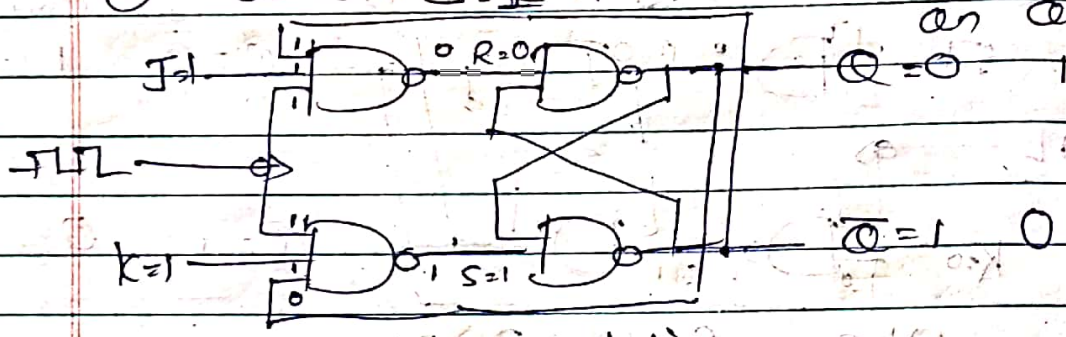
0 0

Set condition

Case 5 J=1 K=1

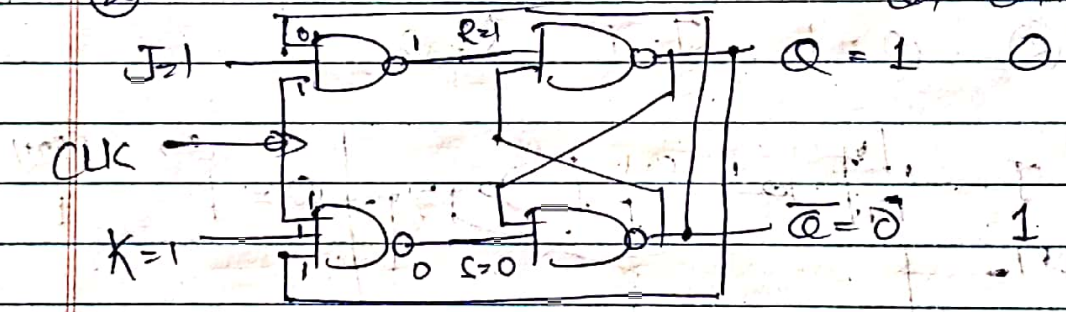


① Q=0 J=1 K=1



Set condition

② Q=1 J=1 K=1



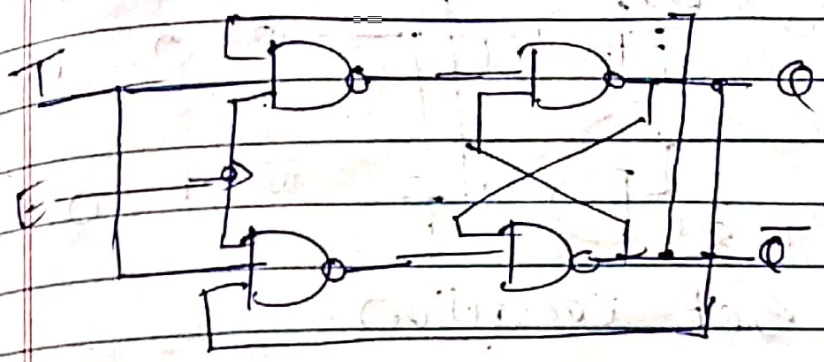
Reset condition

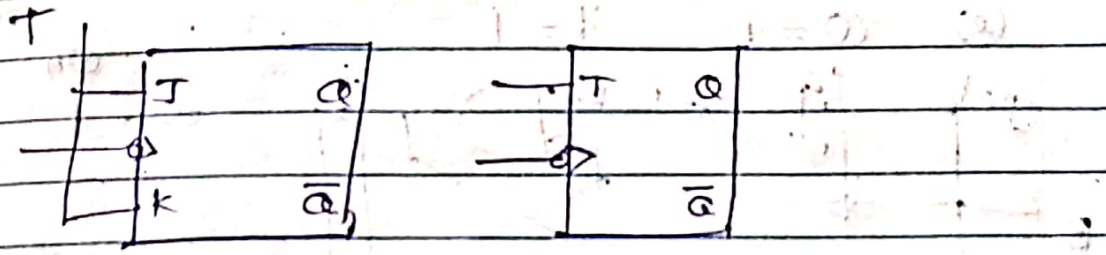
① Q=0 J=1 K=1 Set } Toggle
② Q=1 J=1 K=1 Reset }

E	J	K	Q	Q̄	
0	X	X	Q	Q̄	No change
1	0	0	Q	Q̄	No change
1	0	1	0	1	Reset
1	1	0	1	0	Set
1	1	1	Q̄	Q	Toggle

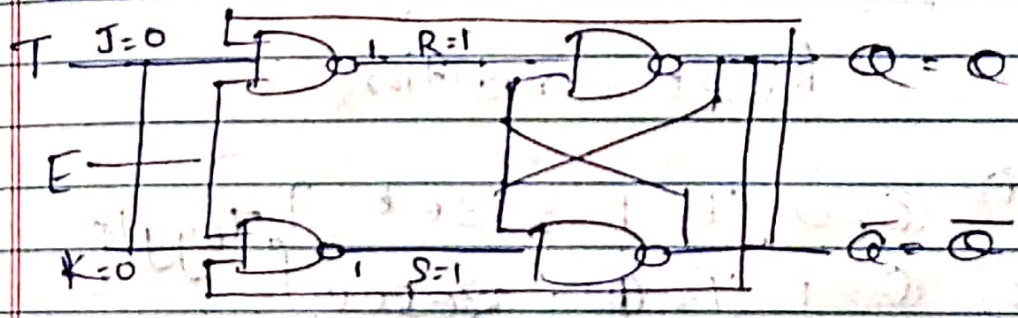
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TFT (Toggle flip flop)



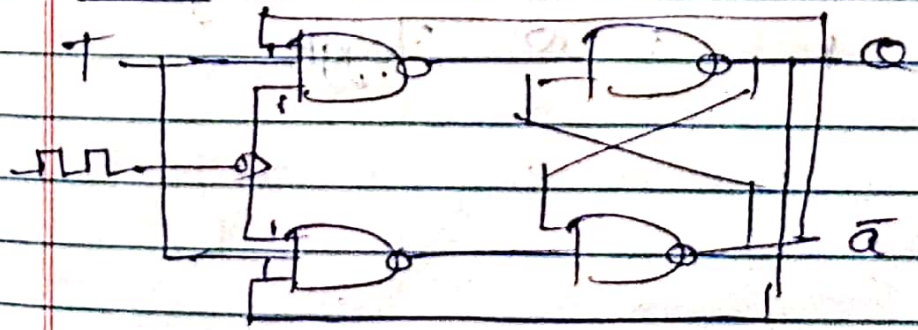


Case 1 E = 1 T = 0



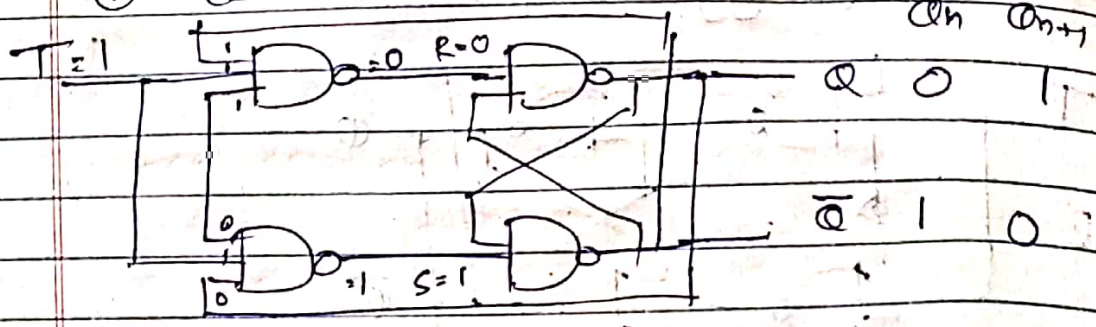
No change

Case 2 E = 1 T = 1



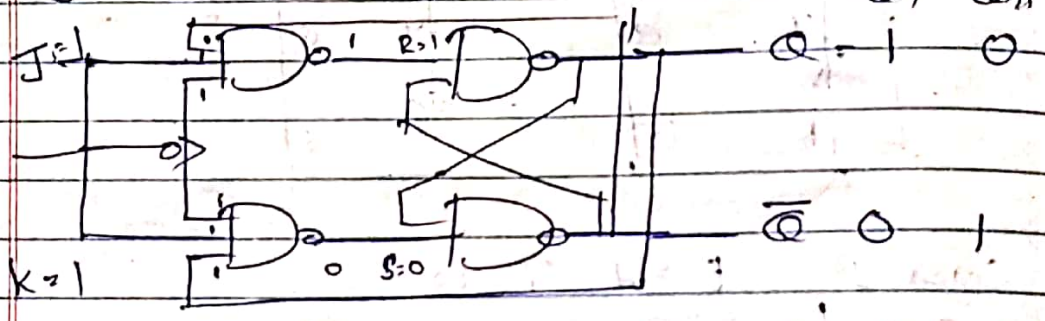
Scanned with CamScanner

① $Q=0$ $T=1$



Set condition

② $Q=1$ $T=1$



Reset condition

① $Q=0$ $T=1$ → set
② $Q=1$ $T=0$ → Reset
} Toggle

E	T	Q	$\bar{Q}$	
1	0	Q	$\bar{Q}$	No change
1	1	$\bar{Q}$	Q	Toggle

Scanned with CamScanner

Truth Table

SR Latch

S	R	Q	$\bar{Q}$	
0	0	X	X	RACE
0	1	0	1	RESET
1	0	1	0	SET
1	1	Q	$\bar{Q}$	Nochange

SR FF

S	R	Q	$\bar{Q}$	
0	0	Q	$\bar{Q}$	Nochange
0	1	0	1	RESET
1	0	1	0	SET
1	1	X	X	RACE

DFF

D	Q	$\bar{Q}$	
0	0	1	RESET
1	1	0	SET

TFF

T	Q	$\bar{Q}$	
0	Q	$\bar{Q}$	Nochange
1	$\bar{Q}$	Q	Toggle

JK FF

J	K	Q	$\bar{Q}$	
0	0	Q	$\bar{Q}$	Nochange
0	1	0	1	RESET
1	0	1	0	SET
1	1	$\bar{Q}$	Q	Toggle

Scanned with CamScanner

Excitation Table

S R Q $\bar{Q}$
0 0 Q $\bar{Q}$
0 1 0 1
1 0 1 0
1 1 x x

excitation table shows that minimum i/p that are necessary to generate next state when current state is known.

Present		Next	
S	R	Q_n	$\bar{Q}_n$	Q_{n+1}	$\bar{Q}_{n+1}$
0	0	0	1	0	1
0	0	1	0	1	0
0	1	0	1	0	1
0	1	1	0	0	1
1	0	0	1	1	0
1	0	1	0	1	0
1	1	0	0	X	X
1	1	1	1	X	X

Present	Next	S	R	
0	0	0	X	□
0	1	1	0	△
1	0	0	1	○
1	1	X	0	⌂

Scanned with CamScanner

Excitation Table of DFF

	Present	Next	
D	Q_n	$\bar{Q}_n$	Q_{n+1} $\quad$ $\bar{Q}_{n+1}$
0	0	1	0 1
	1	0	0 1
1	0	1	1 0
	1	0	1 0

Excitation Table

Present	Next	
Q_n	Q_{n+1}	D
0	0	0
0	1	1
1	0	0
1	1	1

Excitation Table of T-FF

	Present		Next	
T	Q_n	$\bar{Q}_n$	Q_{n+1}	$\bar{Q}_{n+1}$
0	0	0	0	1
	1	0	1	0
1	0	1	1	0
	1	0	0	1

Excitation Table

Present	Next	
Q_n	Q_{n+1}	T
0	0	0
0	1	1
1	0	1
1	1	0

Scanned with CamScanner

Excitation Table of JKFF

		Present		Next	
J	K	Q_n	$\overline{Q_n}$	Q_{n+1}	$\overline{Q_{n+1}}$
0	0	0	1	0	1
		1	0	1	0
1	0	0	1	1	0
		1	0	1	0
1	1	0	1	1	0
		1	0	0	1

Excitation Table

Present Q_n	Next Q_{n+1}	J	K
0	0	0	X
0	1	1	X
1	0	X	1
1	1	X	0

Excitation Table

Present	Next	S	R
0	0	0	X
0	1	1	0
1	0	0	1
1	1	X	0

Present	Next	D
0	0	0
0	1	1
1	0	0
1	1	1

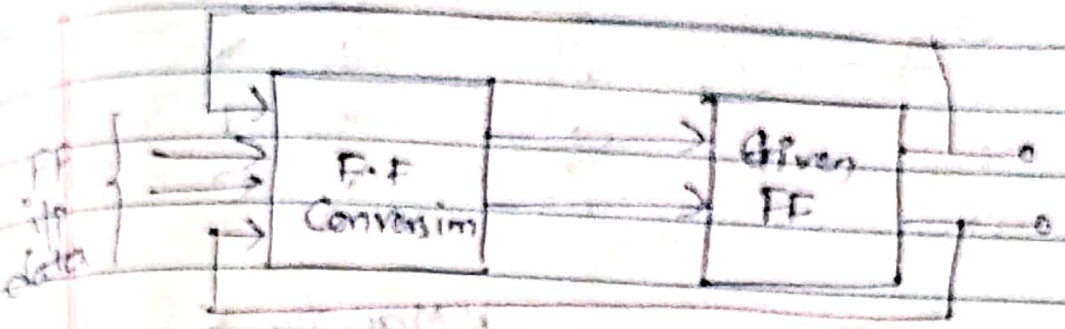
Present	Next	T
0	0	0
0	1	1
1	0	1
1	1	0

Present	Next	J	K
0	0	0	X
0	1	1	X
1	0	X	1
1	1	X	0

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Flip Flop Conversion

To convert One type of FF to another type of FF we use excitation Table & K-Map



Convert SRFF to DFF

D	Present Q_n	Next Q_{n+1}	S	R
0	0	0	0	X
1	0	1	1	0
0	1	0	0	1
1	1	1	X	0

K-Map for S

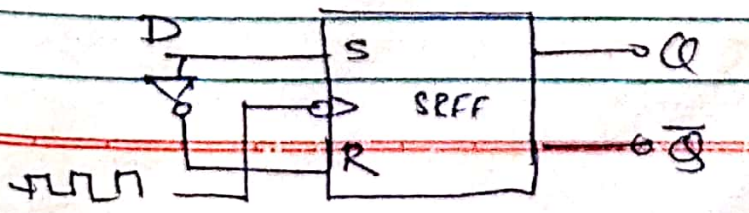
D \ Q_n	Q_n	$\bar{Q}_n$
$\bar{D}$	0 (0)	0 (1)
D	1 (2)	X (3)

$S = D$

K-Map for R

D \ Q_n	$\bar{Q}_n$	Q_n
$\bar{D}$	X (0)	1 (1)
D	0 (2)	Ø (3)

$R = Q_n \bar{D}$



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JKFF TO TFF

T	Present Q_n	Next Q_{n+1}	J	K
0	0	0	0	X
1	0	1	1	X
1	1	0	X	1
0	1	1	X	0

K-Map J

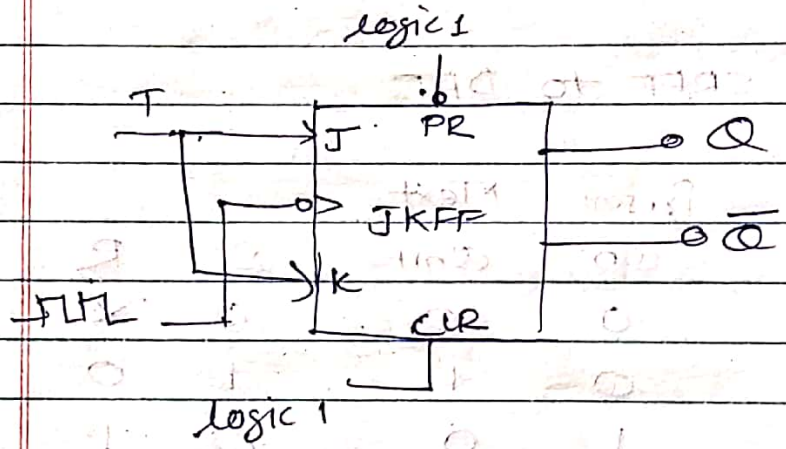
J / Q_n	$\bar{Q}_n$	Q_n
$\bar{T}$	0 (0)	X (1)
T	1 (2)	X (3)

K-Map for K

T / Q_n	Q_n	$\bar{Q}_n$
$\bar{T}$	X (0)	0 (1)
T	X (2)	1 (3)

J = T

K = T



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SRFF TO TFF

T	Present Q_n	Next Q_{n+1}	S	R
0	0	0	0	X
1	0	1	1	0
1	1	0	0	1
0	1	1	X	0

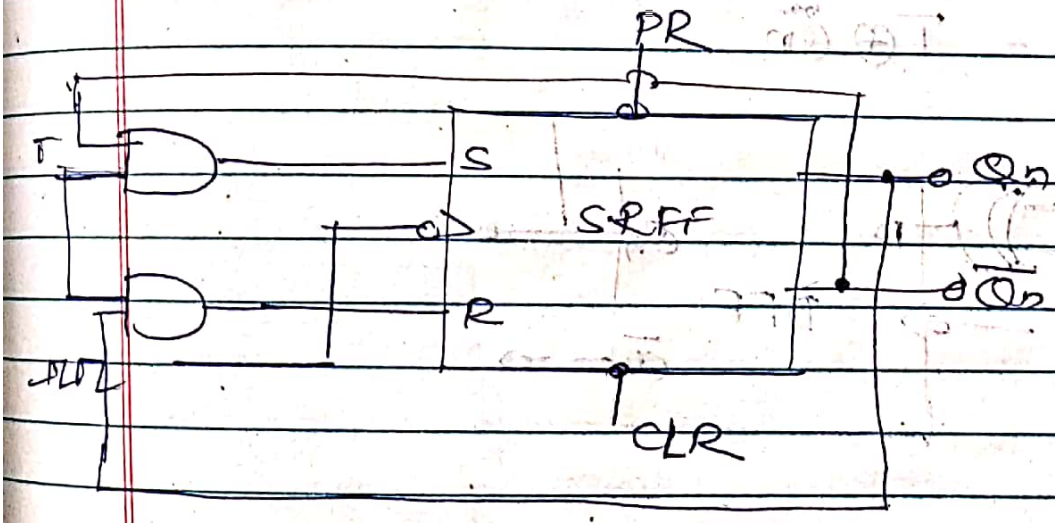
K-Map for S

T \ Q_n	$\bar{Q}_n$	Q_n
$\bar{T}$	0 (1)	X (3)
T	1 (2)	0 (4)

K-Map for R

T \ Q_n	$\bar{Q}_n$	Q_n
$\bar{T}$	X (1)	0 (3)
T	0 (2)	1 (4)

$S = T\bar{Q}_n$ $\quad R = TQ_n$

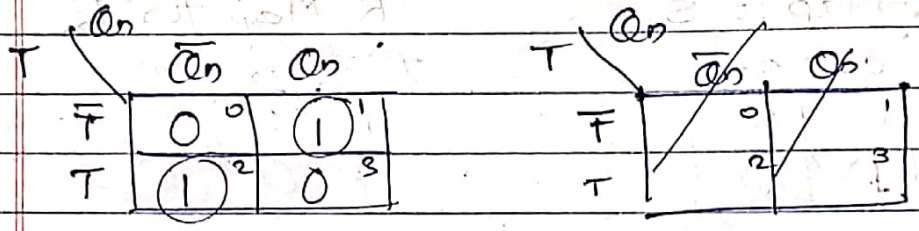


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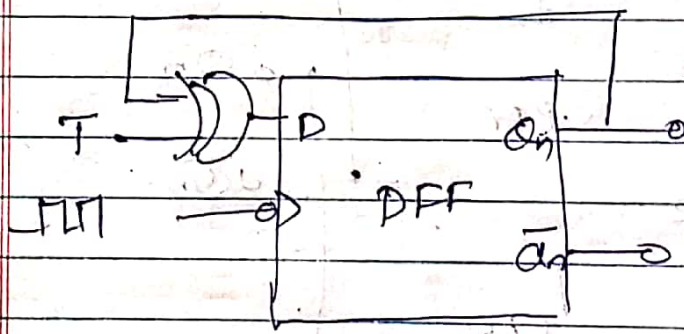
D-FF to TFF

T	Present	Next	D
0	0	0	0
1	0	1	1
1	1	0	0
0	1	1	1

K-Map for D



$$D = T\bar{Q}_n + TQ_n$$
$$= T \oplus \bar{Q}_n$$



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SRFF TO JKFF

	J	K	Present	Next	S	R
0	0	0	0	0	0	X
2	0	1	0	0	0	X
4	1	0	0	1	1	0
6	1	1	0	1	1	0
3	0	1	1	0	0	1
7	1	1	1	0	0	1
1	0	0	1	1	X	0
5	1	0	1	1	X	0

K-Map for S

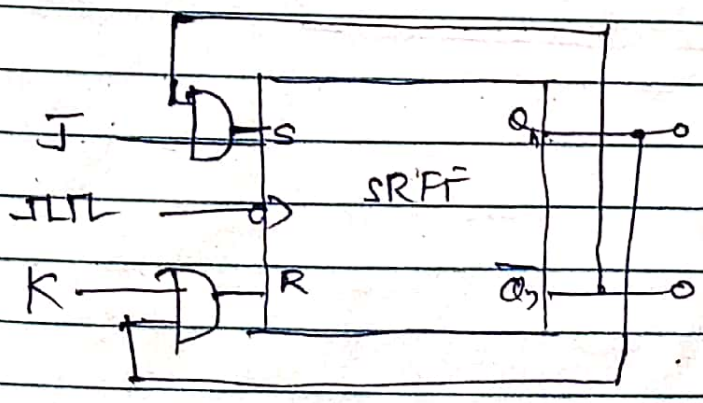
J \ Q_n	$\bar{Q}_n$	Q_n	Q_n	$\bar{Q}_n$
$\bar{J}$	0	X 1	3	2
J	1 4	X 5	7	1 6

$S = J\bar{Q}_n$

K-Map for R

J \ Q_n	$\bar{Q}_n$	$\bar{Q}_n$	Q_n	Q_n
$\bar{J}$	X 0	1	1 3	X 2
J	4	5	1 7	6

$R = K Q_n$



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DFF to SRFF

	S	R	Present	Next	D
0	0	0	0	0	0
2	0	1	0	0	0
4	1	0	0	1	1
4	1	0	0	1	1
3	0	1	1	0	0
3	0	1	1	0	0
1	0	0	1	1	1
5	1	0	1	1	1

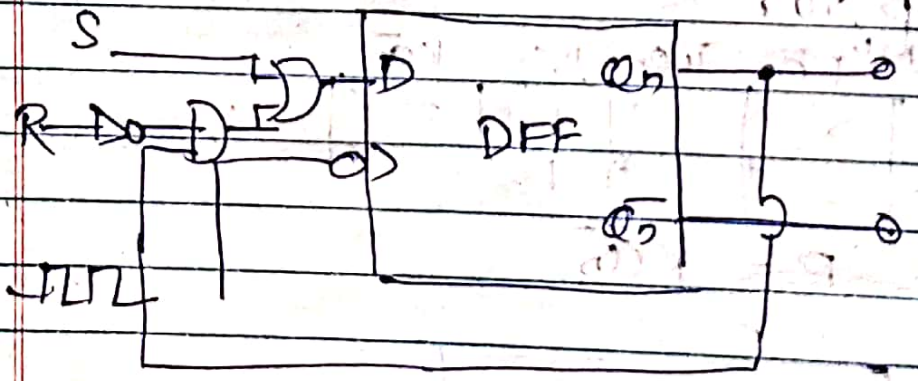
PRS	R	Q
0 0 0	X	0
0 1	0	0
1 0 0	1	
1 1	X	0

PND	
0 0	0
0 1	1
1 0	0
1 1	1

K Map for D

S \ $R\bar{Q}_n$	$\bar{R}\bar{Q}_n$	$\bar{R}Q_n$	RQ_n	$R\bar{Q}_n$
$\bar{S}$	0	1	0	0
S	1	1	X	X

$$D = S + \bar{R}Q_n$$

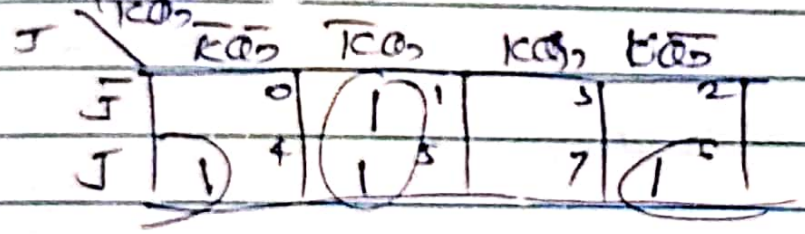


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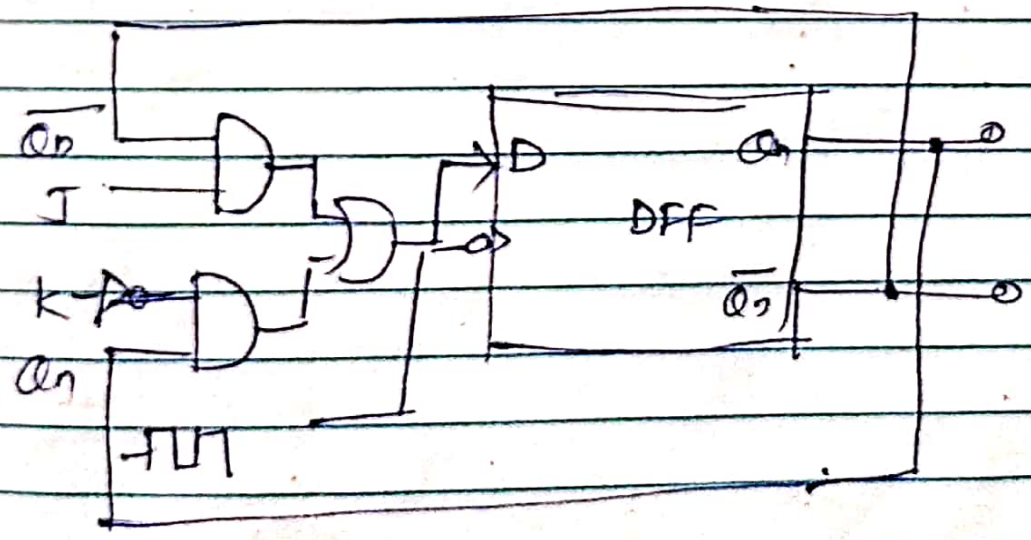
DFF to JKFF

	J	K	Q_n	Q_{n+1}	D
0	0	0	0	0	0
2	0	1	0	0	0
4	1	0	0	1	1
6	1	1	0	1	1
3	0	1	1	0	0
7	1	1	1	0	0
1	0	0	1	1	1
5	1	0	1	1	1

K-Map for D



$$D = J\bar{Q}_n + \bar{K}Q_n$$



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Register

A group or set of flip flop that are used to store binary data is called as Register.

The registers are classified depending on the method data is applied to and outputted from a register.

Types of Register

1. Serial-In - Serial-Out (SISO)
2. Serial-In - Parallel-Out (SIPO)
3. Parallel-In - Serial-Out (PISO)
4. Parallel-In - Parallel-Out (PIPO)

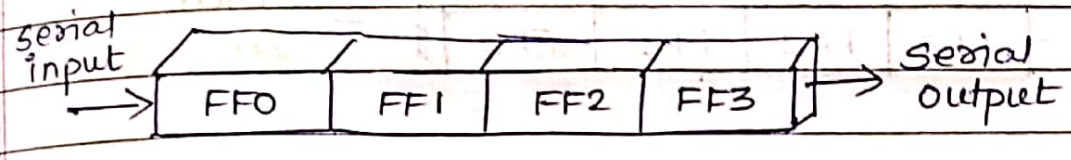
Shift Register

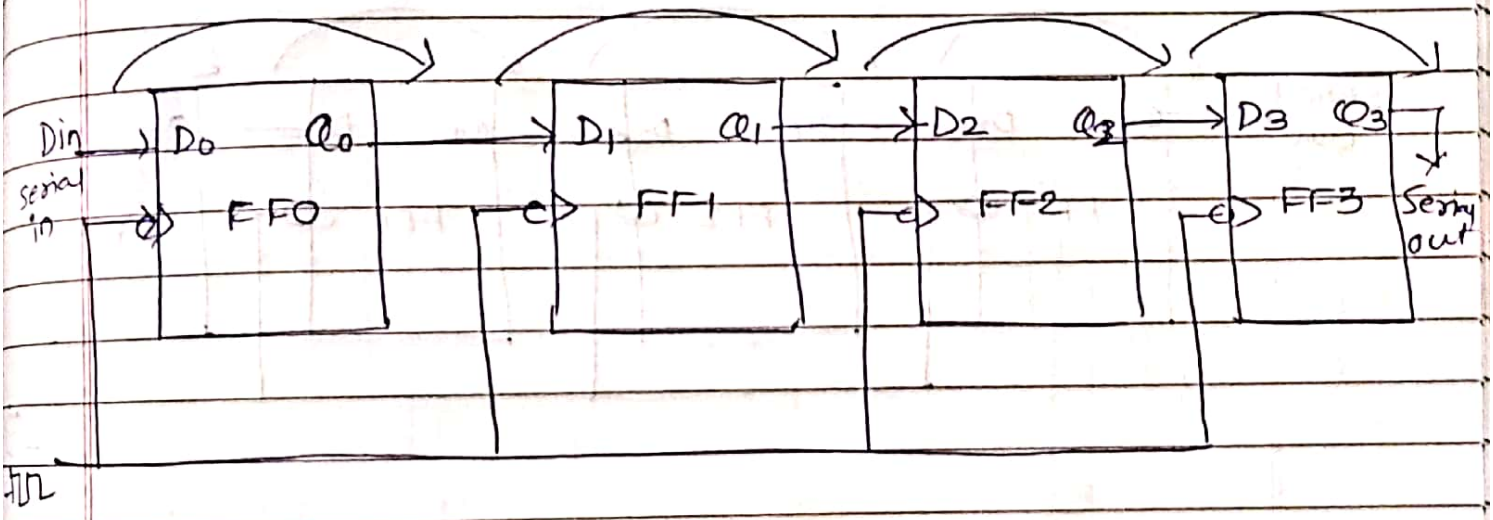
The register in which data can be shifted out from one flip flop to other with application of clock pulses is called as a shift register

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Serial In Serial Out (right shift)

In serial-in-serial-out shift register right shift, the data bits are shifted from left to right by 1 position during each clock cycle.



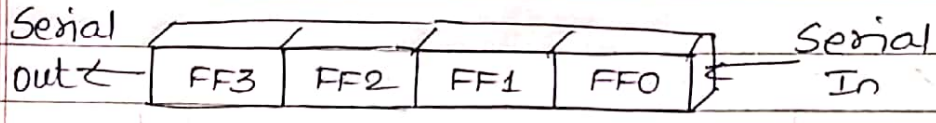


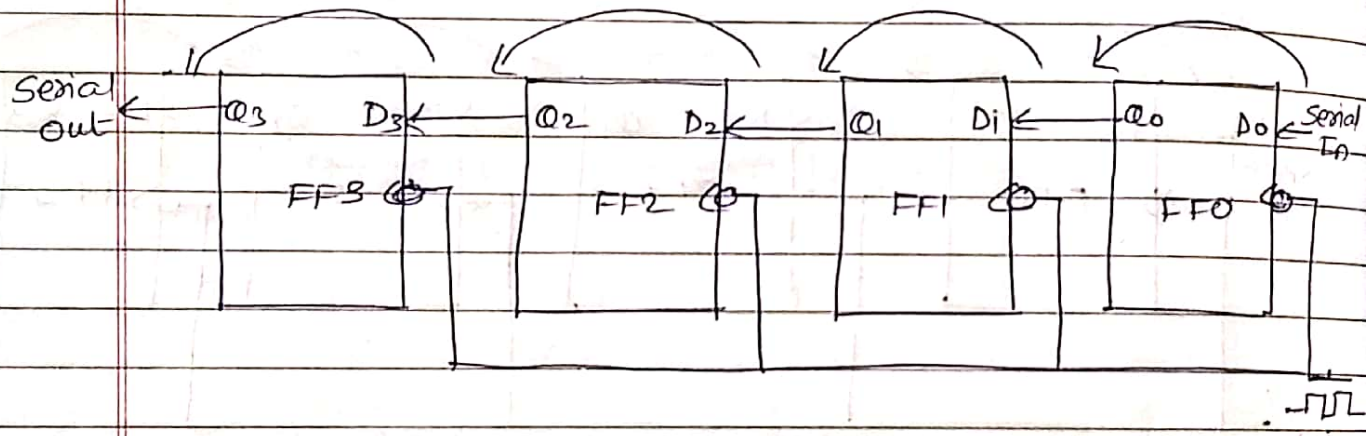
	Q_0	Q_1	Q_2	Q_3	
	0	0	0	0	
Din=1 →	1	0	0	0	1st clock cycle
Din=1 →	1	1	1	1	2nd clock cycle
Din=1 →	1	1	1	1	3rd clock cycle
Din=1 →	1	1	1	1	4th clock cycle

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Serial - In - Serial - out (left Shift)

In the serial-in- serial-out left shift register, the data bits are shifted from right to left by 1 position during each clock cycle.



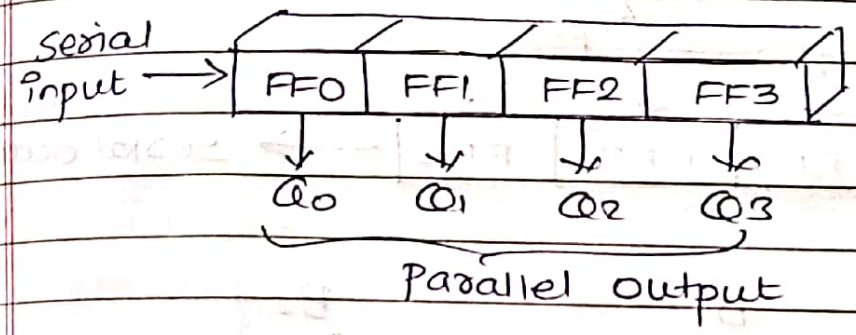


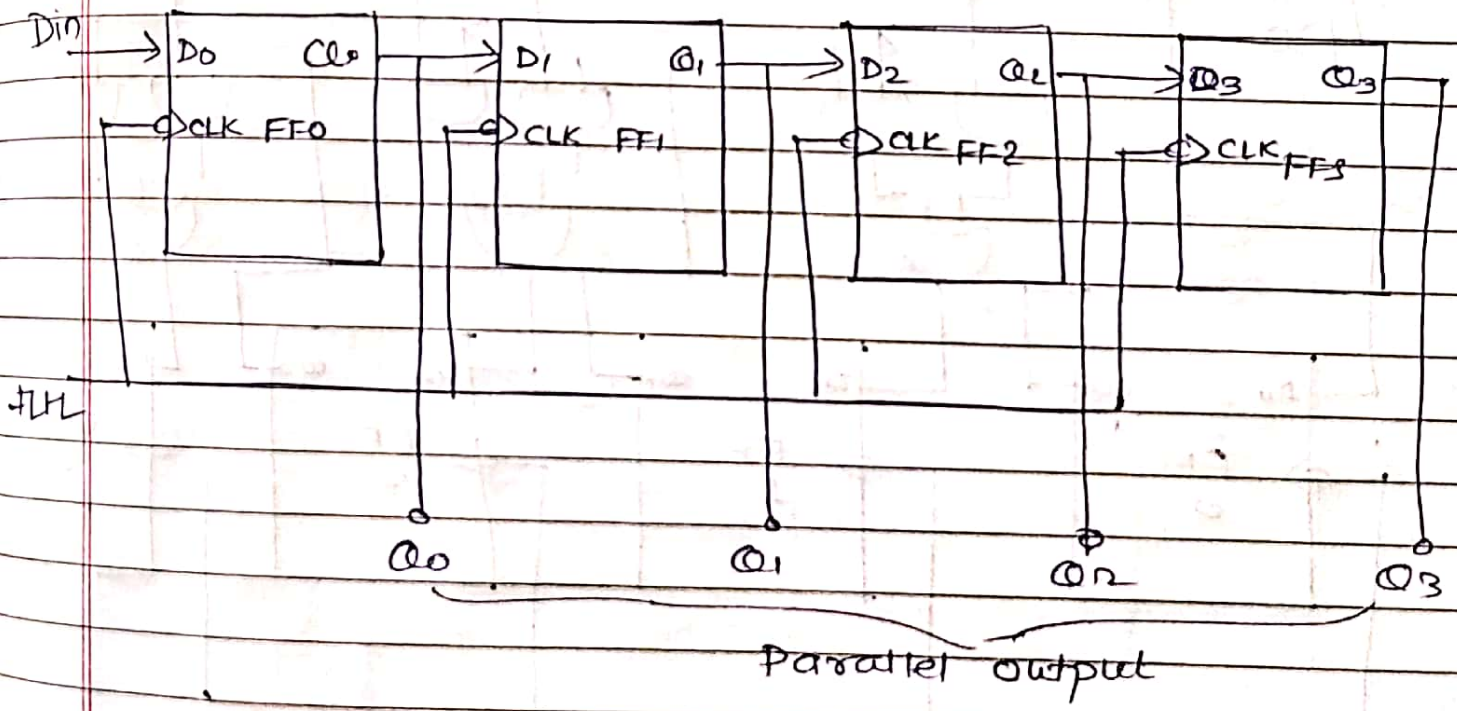
	Q_3	Q_2	Q_1	Q_0	
	0	0	0	0	
1st cycle	0	0	0	1	Din = 1
2nd cycle	0	0	1	1	Din = 1
3rd cycle	0	1	1	1	Din = 1
4th cycle	1	1	1	1	Din = 1

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Serial - In - Parallel - Out shift register

In serial-in-parallel out shift register, all the outputs will be available after 4 clock pulses for a 4 bit shift register.



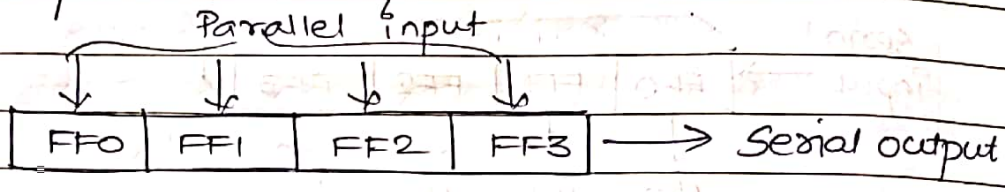


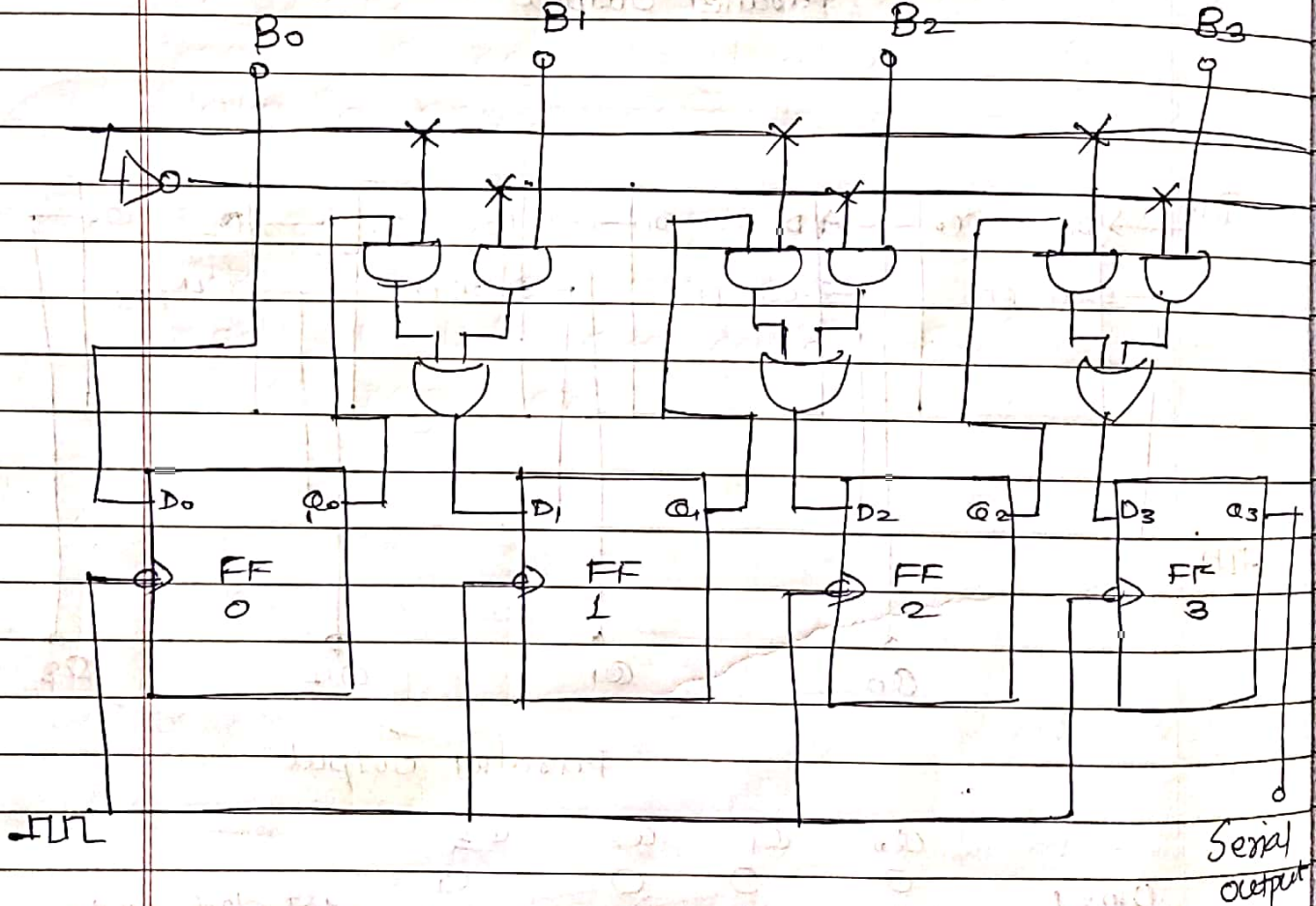
	Q_0	Q_1	Q_2	Q_3	
Din = 1	0 → 1	0 → 0	0 → 0	0 → 0	1st clock cycle
Din = 1	1 → 1	0 → 1	0 → 0	0 → 0	2nd clock cycle
Din = 1	1 → 1	1 → 1	0 → 1	0 → 0	3rd clock cycle
Din = 1	1 → 1	1 → 1	1 → 1	0 → 1	4th clock cycle

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Parallel In Serial Out shift register

In parallel in serial out shift register, all the inputs are simultaneously loaded but the shift register outputs will be bit by bit serially

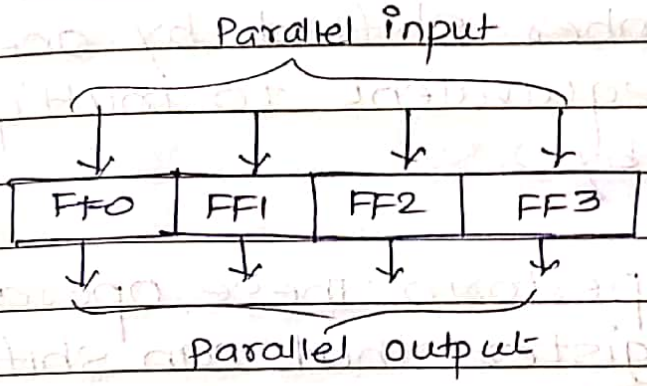


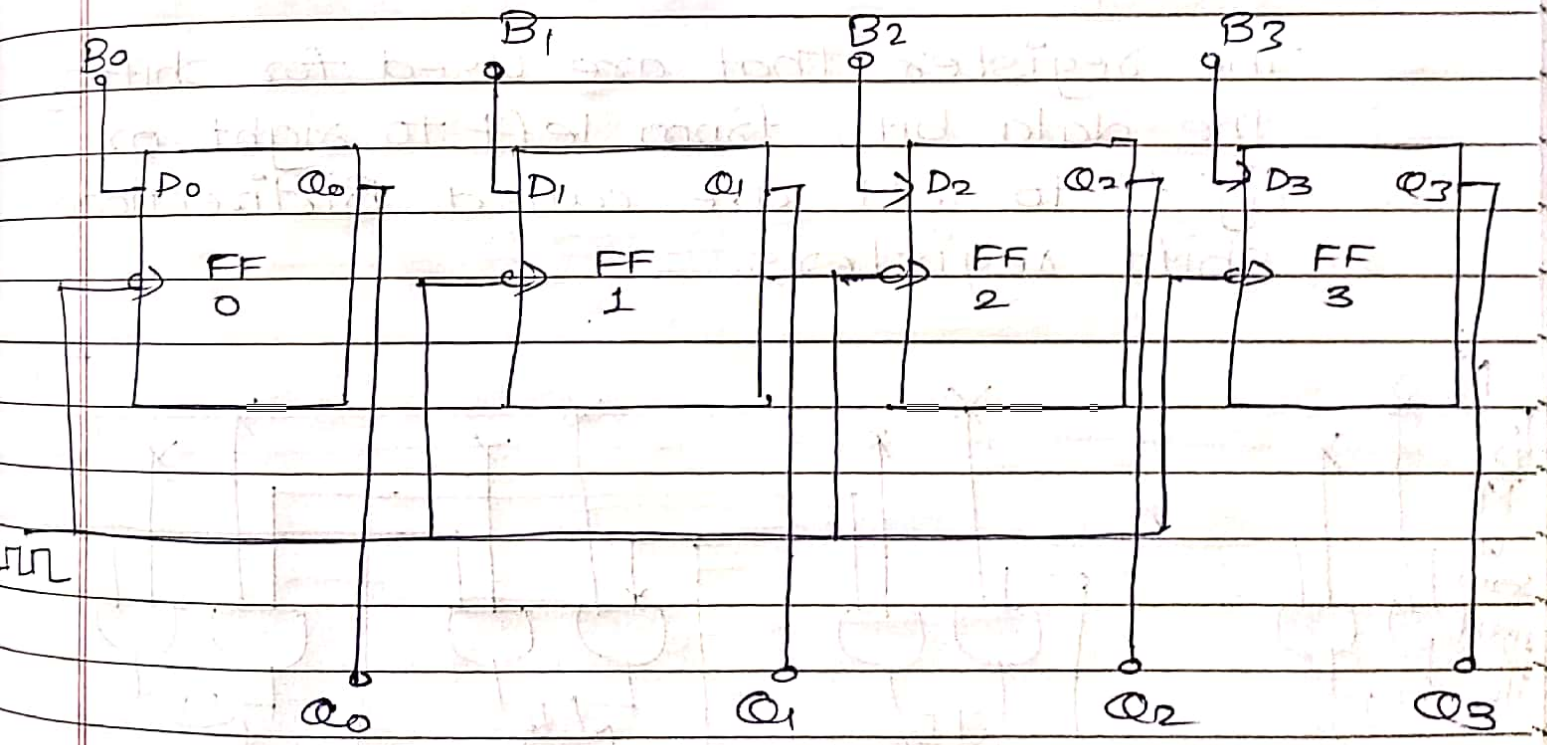


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Parallel In Parallel Out shift register

In Parallel in Parallel out shift register all the shift register inputs are loaded simultaneosly and all the outputs will be available simultaneously.





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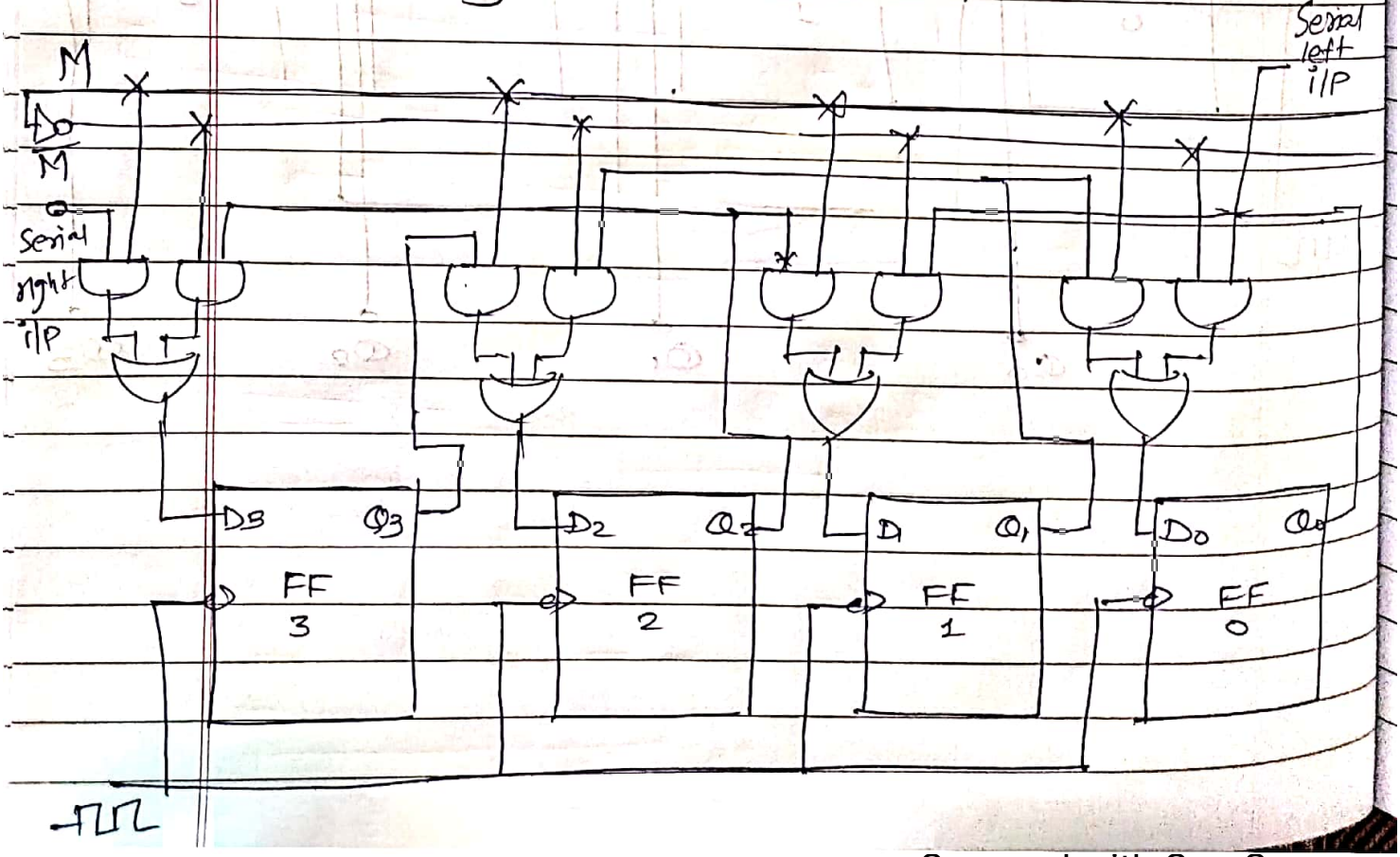
Bidirectional Shift register

A binary number shifted by one bit to the right is equivalent to dividing the number by 2.

A binary number shifted by one bit to the left is equivalent to multiplying the number by 2.

In order to perform these operations, we require a register that can shift the data in any direction.

The register that are used for shifting the data bits from left to right or right to left are called Bidirectional shift registers.



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Applications of Shift Register

① Delay line
A serial in serial out shift register can be used to add delay time.

② Serial to parallel converter
A serial in parallel out shift register can be used to convert data in the serial form to parallel form.

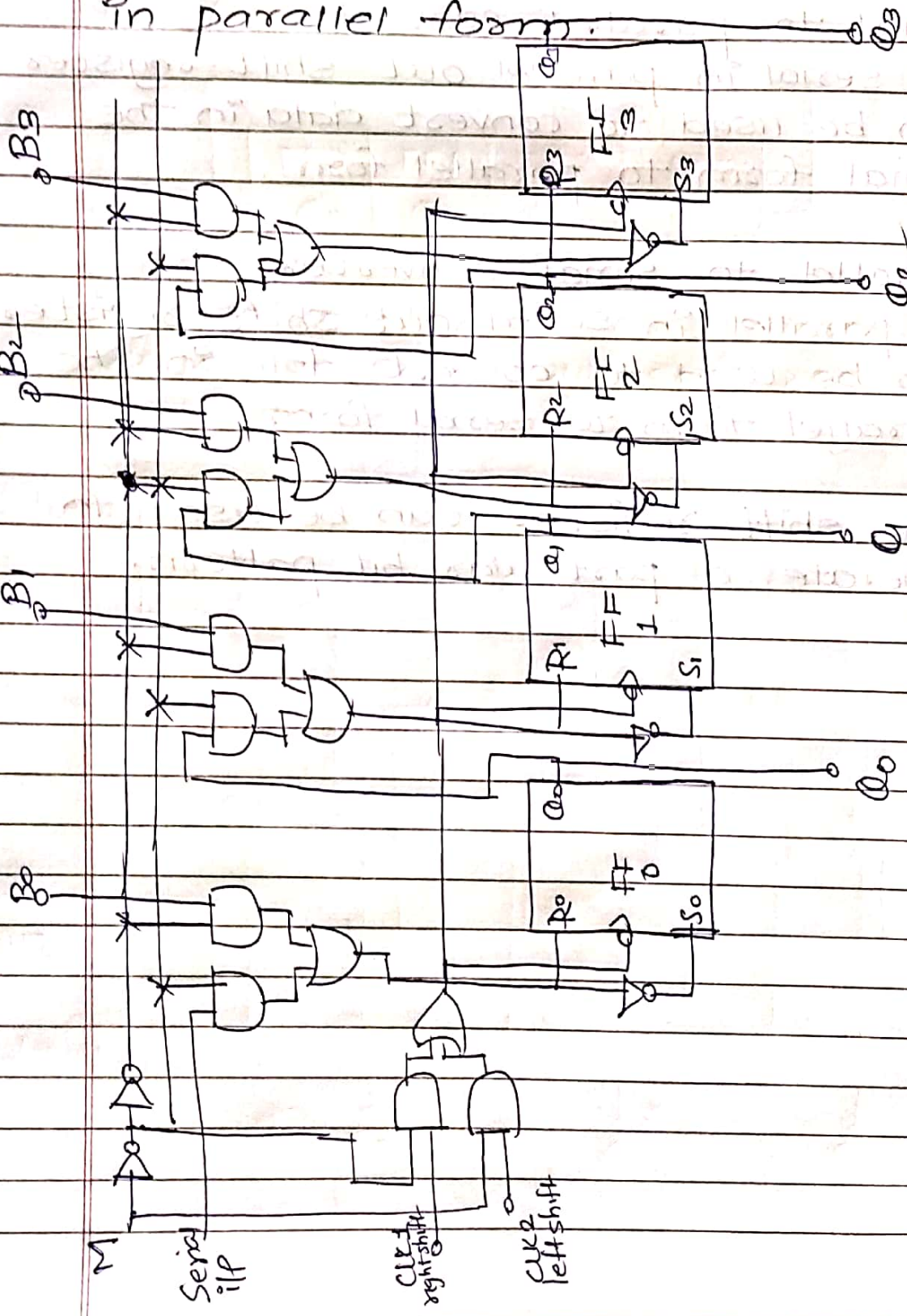
③ Parallel to serial converter
A parallel in serial out shift register can be used to convert data in the parallel form to serial form

④ The shift register can be used to generate a particular bit pattern.

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Universal Shift Register

A universal shift register is a bidirectional register, whose input can be either in serial form or in parallel form and whose output can also be either in serial form or in parallel form.

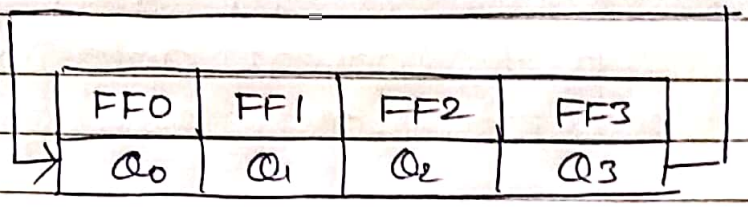


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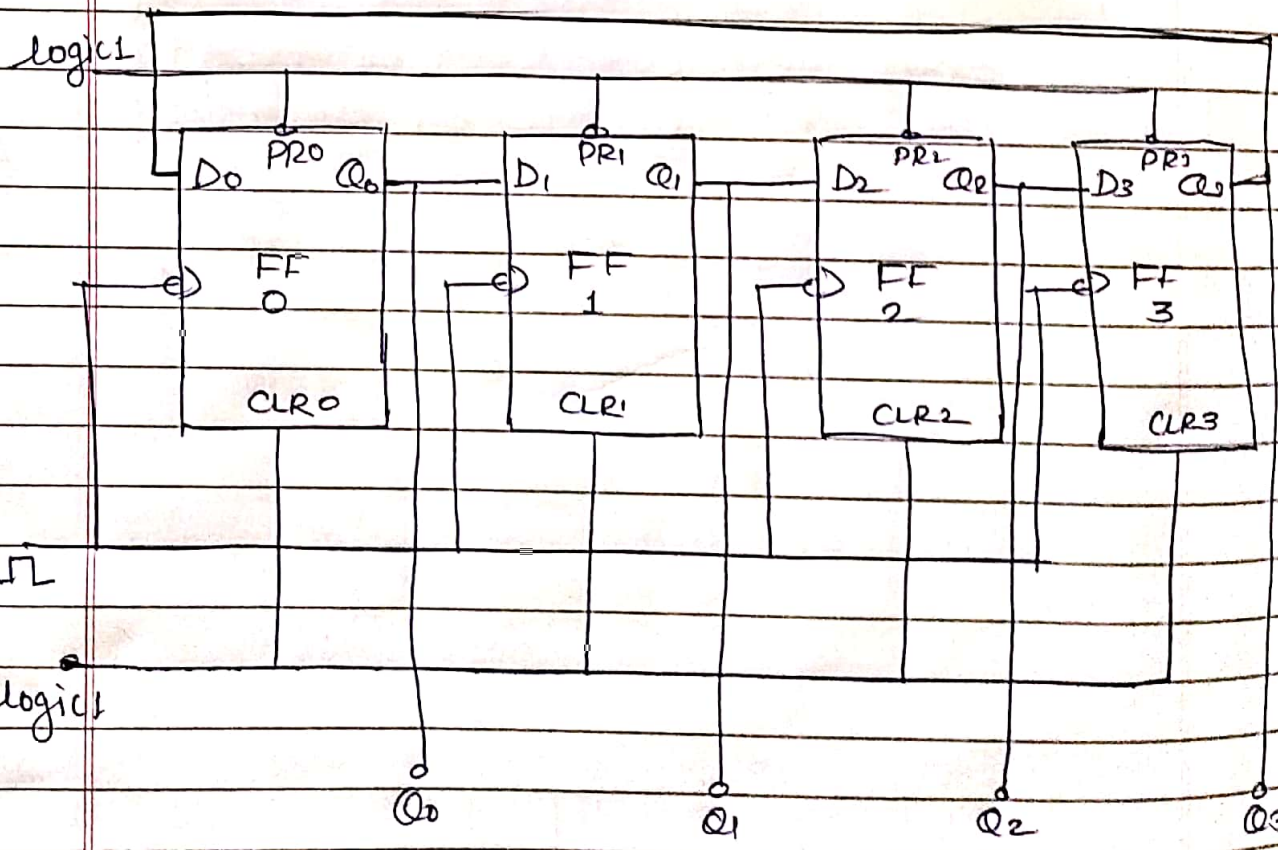
RING Counter

Ring counter is a synchronous shift register counter.

In a ring counter the output of the last flip flop is connected to the first flip flop.



A ring counter is constructed by using serial in serial out shift register and feedback.

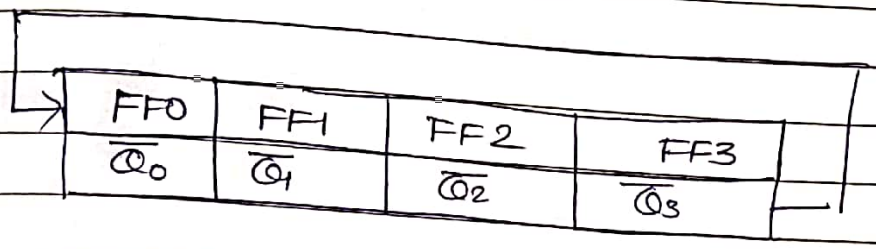


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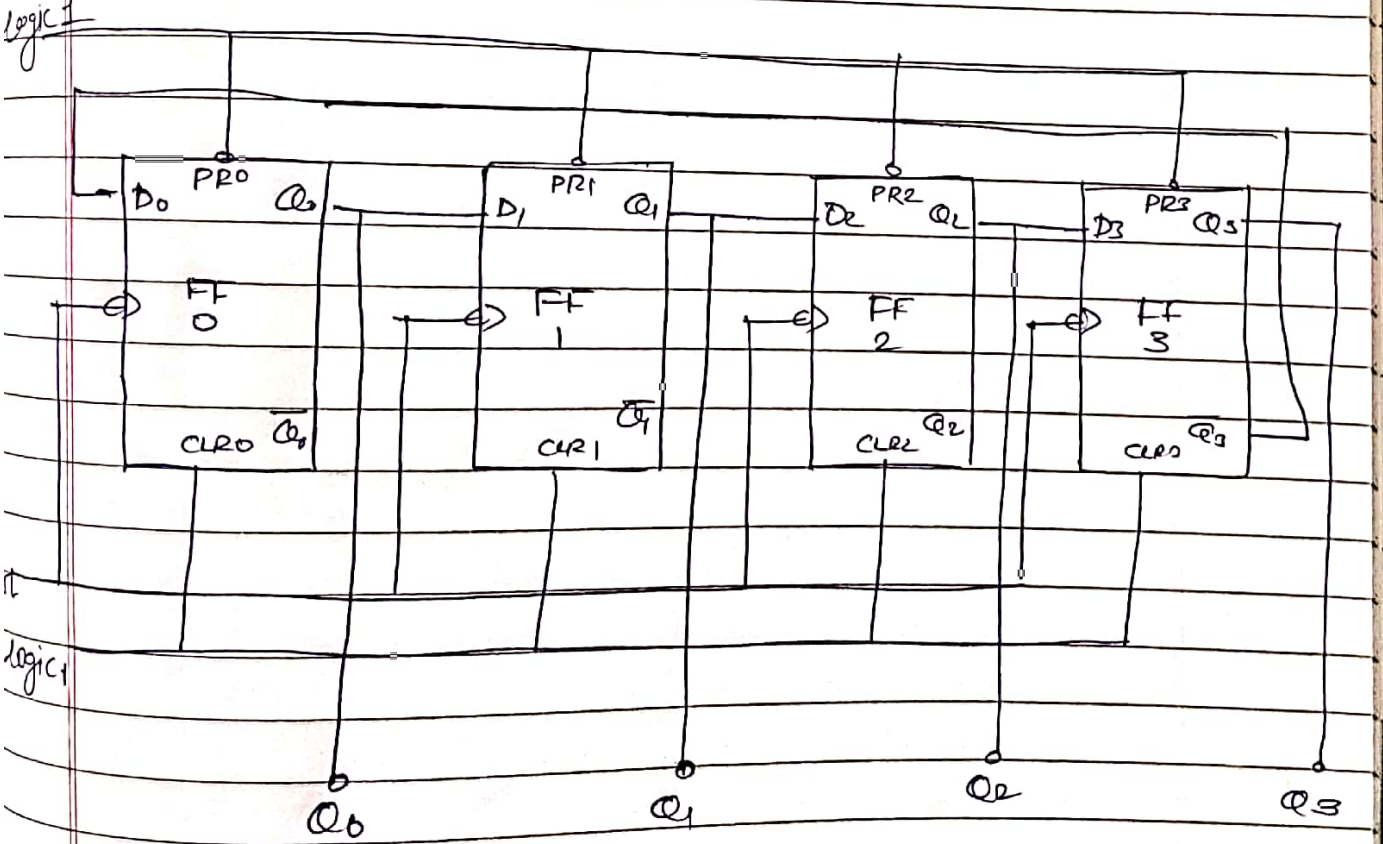
Twisted Ring counter / Johnson Counter

In a ring counter Q output of the last flip flop is connected to the first flip flop.

But in twisted ring counter $\overline{Q}$ output of last flip flop is connected to the first flip flop.



Twisted Ring counter is also known as Johnson Counter.



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