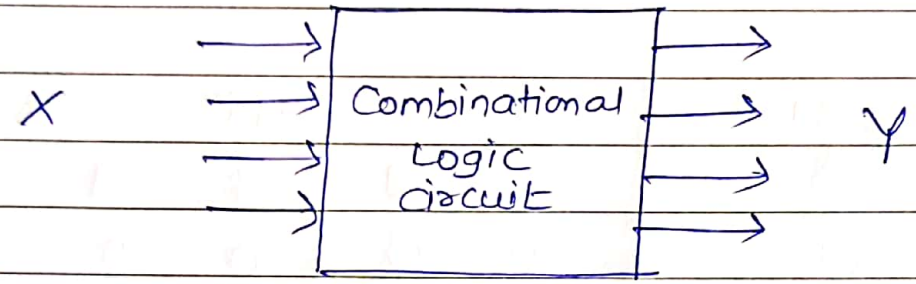
Combinational logic circuits

Combinational logic circuits are the circuits whose output depends on it's present input only

Block diagram



A combinational circuit performs an operati based on:

1. Truth Table
2. Boolean expression
3. Logic diagram

Examples

1. Half Adder
2. Full Adder
3. Half subtractor
4. Full subtractor
5. Binary Adder
6. BCD adder
7. Multiplexer
8. Demultiplexer

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classmate
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Code Converters

1. Binary to gray code converter
2. Gray to binary code converter
3. Binary to BCD code converter
4. BCD to Excess-3 code converter

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Dec 2017, 06 M

Design & implement binary to gray code converter using logic gates

Binary to Gray



Truth Table

	i/p				o/p			
	B_3	B_2	B_1	B_0	G_3	G_2	G_1	G_0
0	0	0	0	0	0	0	0	0
1	0	0	0	1	0	0	0	1
2	0	0	1	0	0	0	1	1
3	0	0	1	1	0	0	1	0
4	0	1	0	0	0	1	1	0
5	0	1	0	1	0	1	1	1
6	0	1	1	0	0	1	0	1
7	0	1	1	1	0	1	0	0
8	1	0	0	0	1	1	0	0
9	1	0	0	1	1	1	0	1
10	1	0	1	0	1	1	1	1
11	1	0	1	1	1	1	1	0
12	1	1	0	0	1	0	1	0
13	1	1	0	1	1	0	1	1
14	1	1	1	0	1	0	0	1
15	1	1	1	1	1	0	0	0

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K-Map for G3

B_3B_2 \ B_1B_0	$\bar{B}_1\bar{B}_0$	$\bar{B}_1B_0$	B_1B_0	$B_1\bar{B}_0$
$\bar{B}_3\bar{B}_2$	0	1	3	2
$\bar{B}_3B_2$	4	5	7	6
B_3B_2	1 (12)	1 (13)	1 (15)	1 (14)
$B_3\bar{B}_2$	1 (8)	1 (9)	1 (11)	1 (10)

(1)

$G_3 = B_3$

K-Map fo G2

B_3B_2 \ B_1B_0	$\bar{B}_1\bar{B}_0$	$\bar{B}_1B_0$	B_1B_0	$B_1\bar{B}_0$
$\bar{B}_3\bar{B}_2$	0	1	3	2
$\bar{B}_3B_2$	1 (4)	1 (5)	1 (7)	1 (6)
B_3B_2	12	13	15	14
$B_3\bar{B}_2$	1 (8)	1 (9)	1 (11)	1 (10)

(1), (2)

$G_2 = \bar{B}_3B_2 + B_3\bar{B}_2$

$= B_3 \oplus B_2$

K-Map G1

B_3B_2 \ B_1B_0	$\bar{B}_1\bar{B}_0$	$\bar{B}_1B_0$	B_1B_0	$B_1\bar{B}_0$
$\bar{B}_3\bar{B}_2$	0	1	1 (3)	1 (2)
$\bar{B}_3B_2$	1 (4)	1 (5)	7	6
$B_3\bar{B}_2$	1 (12)	1 (13)	15	14
B_3B_2	8	9	1 (11)	1 (10)

(1), (2)

$G_1 = B_2\bar{B}_1 + \bar{B}_1B_2$

$= B_2 \oplus B_1$

K-Map for G0

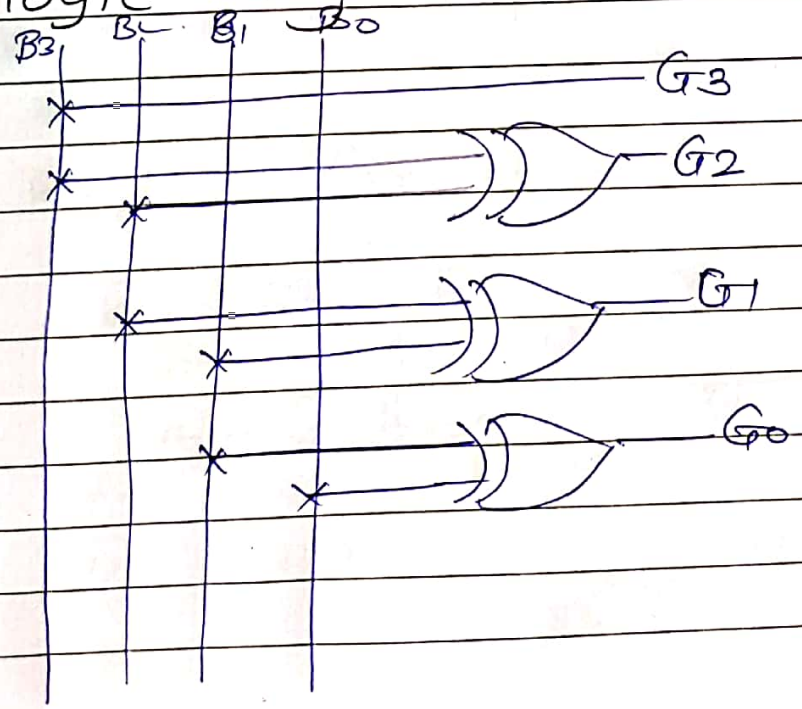
B_3B_2 \ B_1B_0	$\bar{B}_1\bar{B}_0$	$\bar{B}_1B_0$	B_1B_0	$B_1\bar{B}_0$
$\bar{B}_3\bar{B}_2$	0	1 (1)	3	1 (2)
$\bar{B}_3B_2$	4	1 (5)	7	1 (6)
B_3B_2	12	1 (13)	15	1 (14)
$B_3\bar{B}_2$	8	1 (9)	11	1 (10)

(1), (2)

$G_0 = \bar{B}_1B_0 + B_0\bar{B}_1$

$= B_1 \oplus B_0$

logic diagram



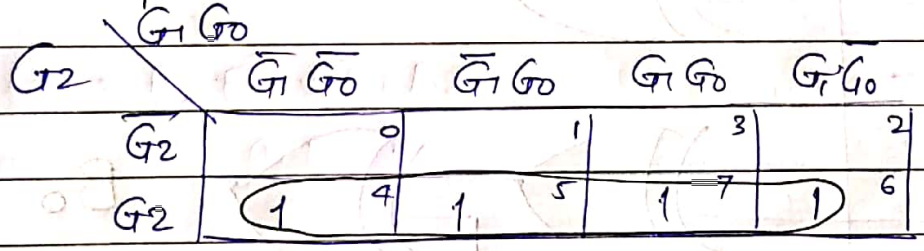
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Design 3 bit gray to binary converter

Truth Table

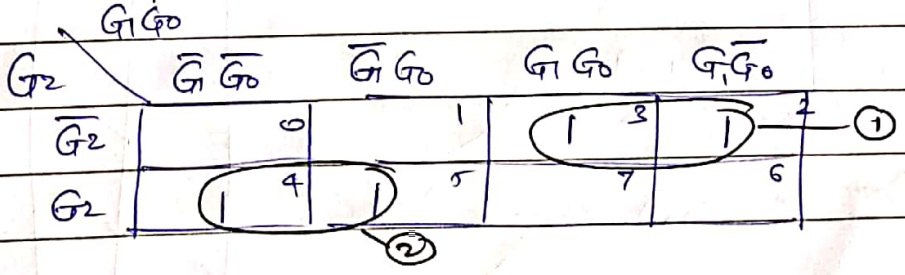
	i/p			o/p		
	G_2	G_1	G_0	B_2	B_1	B_0
0	0	0	0	0	0	0
1	0	0	1	0	0	1
2	0	1	0	0	1	1
3	0	1	1	0	1	0
4	1	0	0	1	1	1
5	1	0	1	1	1	0
6	1	1	0	1	0	0
7	1	1	1	1	0	1

KMap for B2



$$B_2 = G_2$$

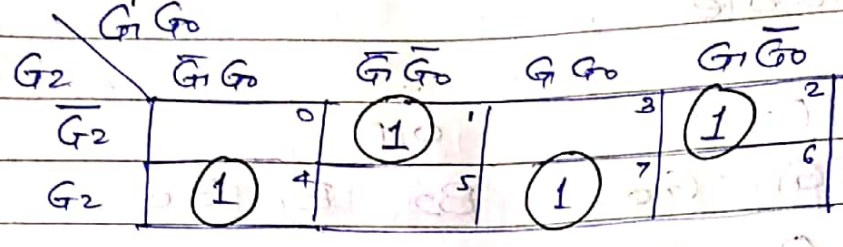
K-Map for B_1



$$B_1 = G_2\bar{G}_1 + \bar{G}_2G_1$$
$$= G_2 \oplus G_1$$

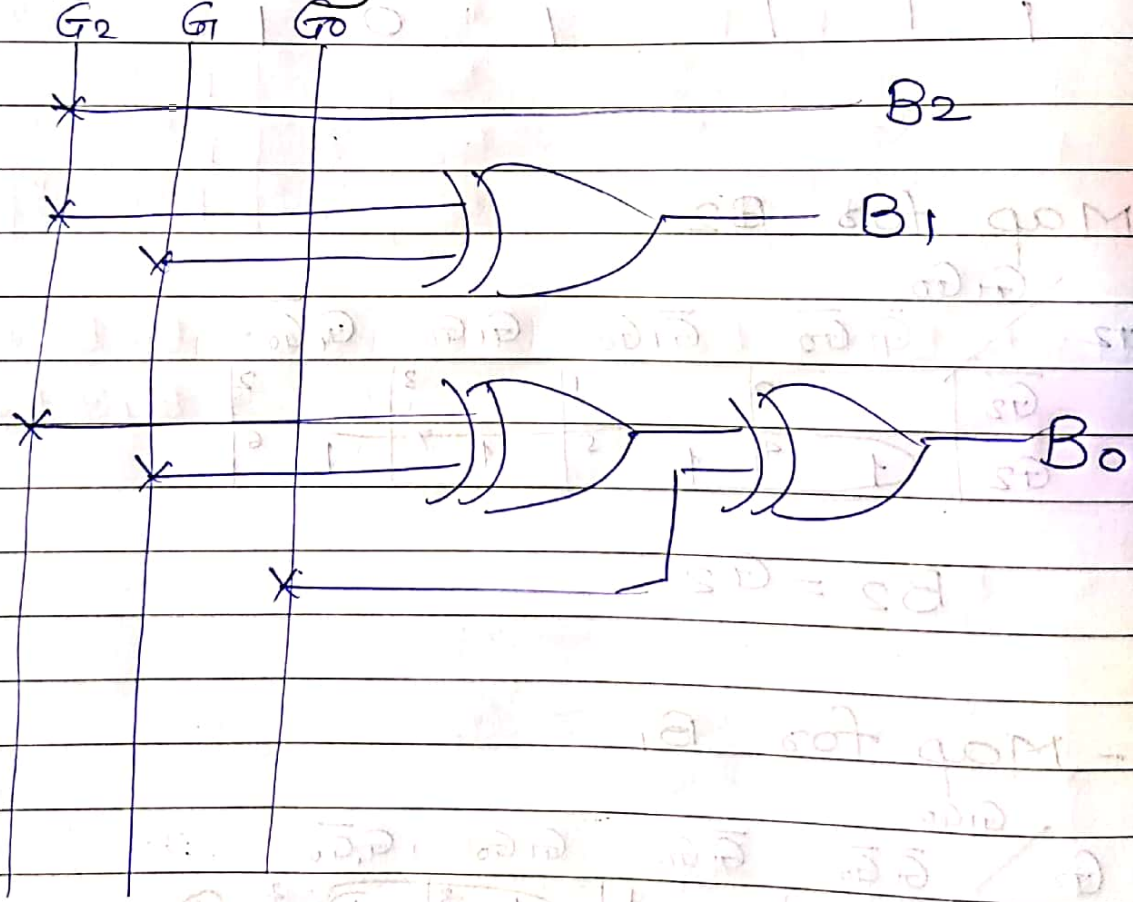
Scanned with CamScanner

K-Map for B_0



$$B_0 = \bar{G}_2\bar{G}_1G_0 + \bar{G}_2G_1\bar{G}_0 + G_2\bar{G}_1\bar{G}_0 + G_2G_1G_0$$
$$= \bar{G}_2(\bar{G}_1G_0 + G_1\bar{G}_0) + G_2(\bar{G}_1\bar{G}_0 + G_1G_0)$$
$$= \bar{G}_2(G_1 \oplus G_0) + G_2(\overline{G_1 \oplus G_0})$$
$$= G_2 \oplus G_1 \oplus G_0$$

logic diagram



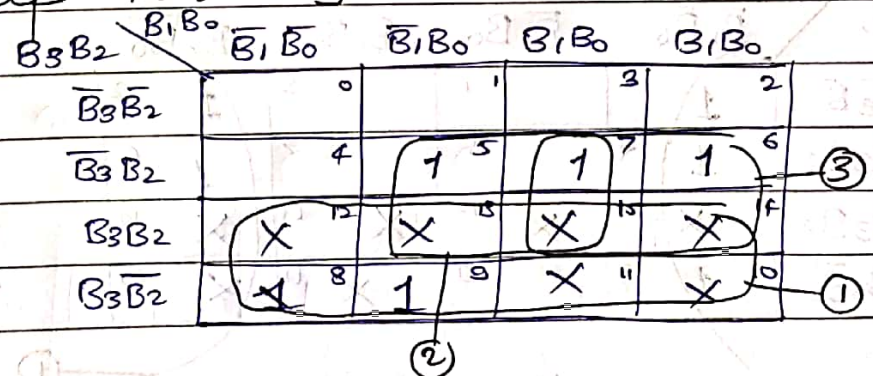
Scanned with CamScanner

Design 4 bit BCD to XS-3 code converter

Truth Table

	i/p				o/p			
	B_3	B_2	B_1	B_0	E_3	E_2	E_1	E_0
0	0	0	0	0	0	0	1	1
1	0	0	0	1	0	1	0	0
2	0	0	1	0	0	1	0	1
3	0	0	1	1	0	1	1	0
4	0	1	0	0	0	1	1	1
5	0	1	0	1	1	0	0	0
6	0	1	1	0	1	0	0	1
7	0	1	1	1	1	0	1	0
8	1	0	0	0	1	0	1	1
9	1	0	0	1	1	1	0	0
10	X	X	X	X	X	X	X	X
11	X	X	X	X	X	X	X	X
12	X	X	X	X	X	X	X	X
13	X	X	X	X	X	X	X	X
14	X	X	X	X	X	X	X	X
15	X	X	X	X	X	X	X	X

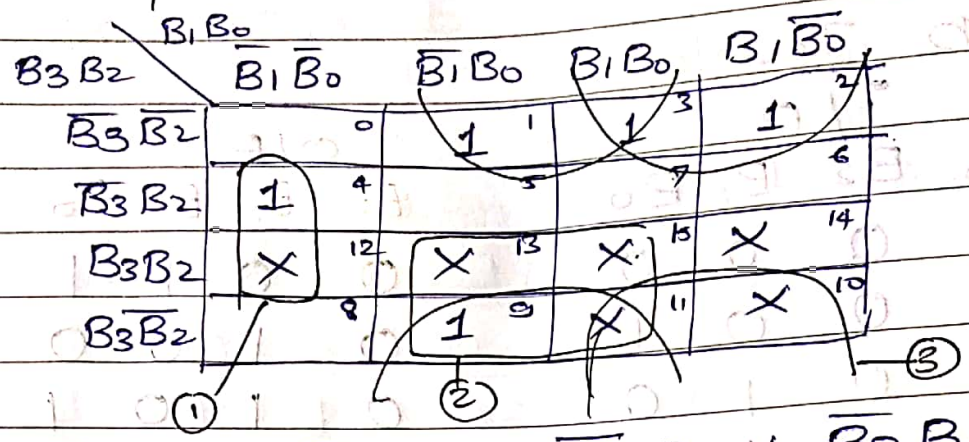
Kmap for E_3



$E_3 = B_3 + B_2B_0 + B_2B_1$

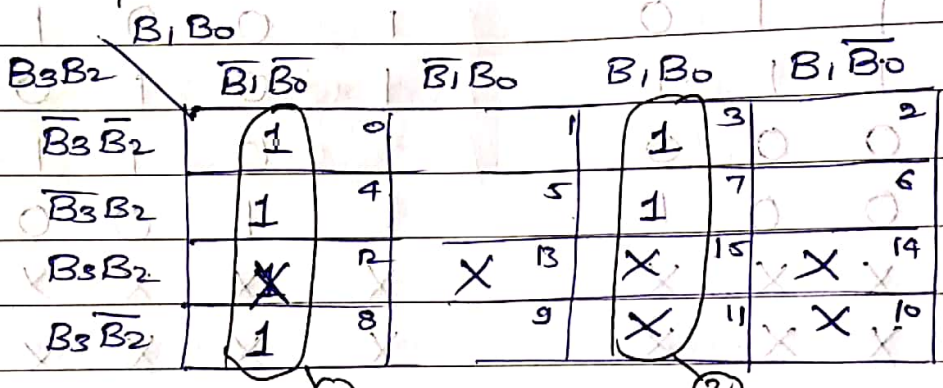
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K-Map for E_2



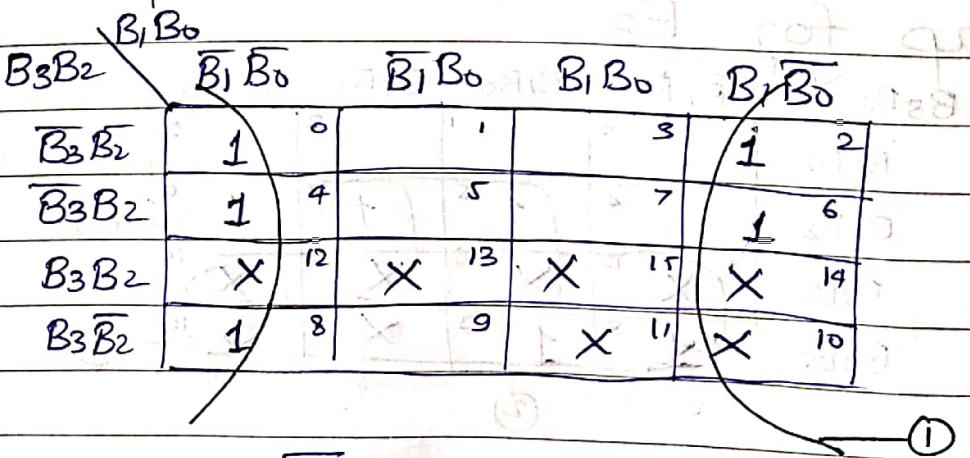
$$E_2 = B_2\bar{B_1}B_0 + \bar{B_2}B_0 + \bar{B_2}B_1$$

K-Map for E_1



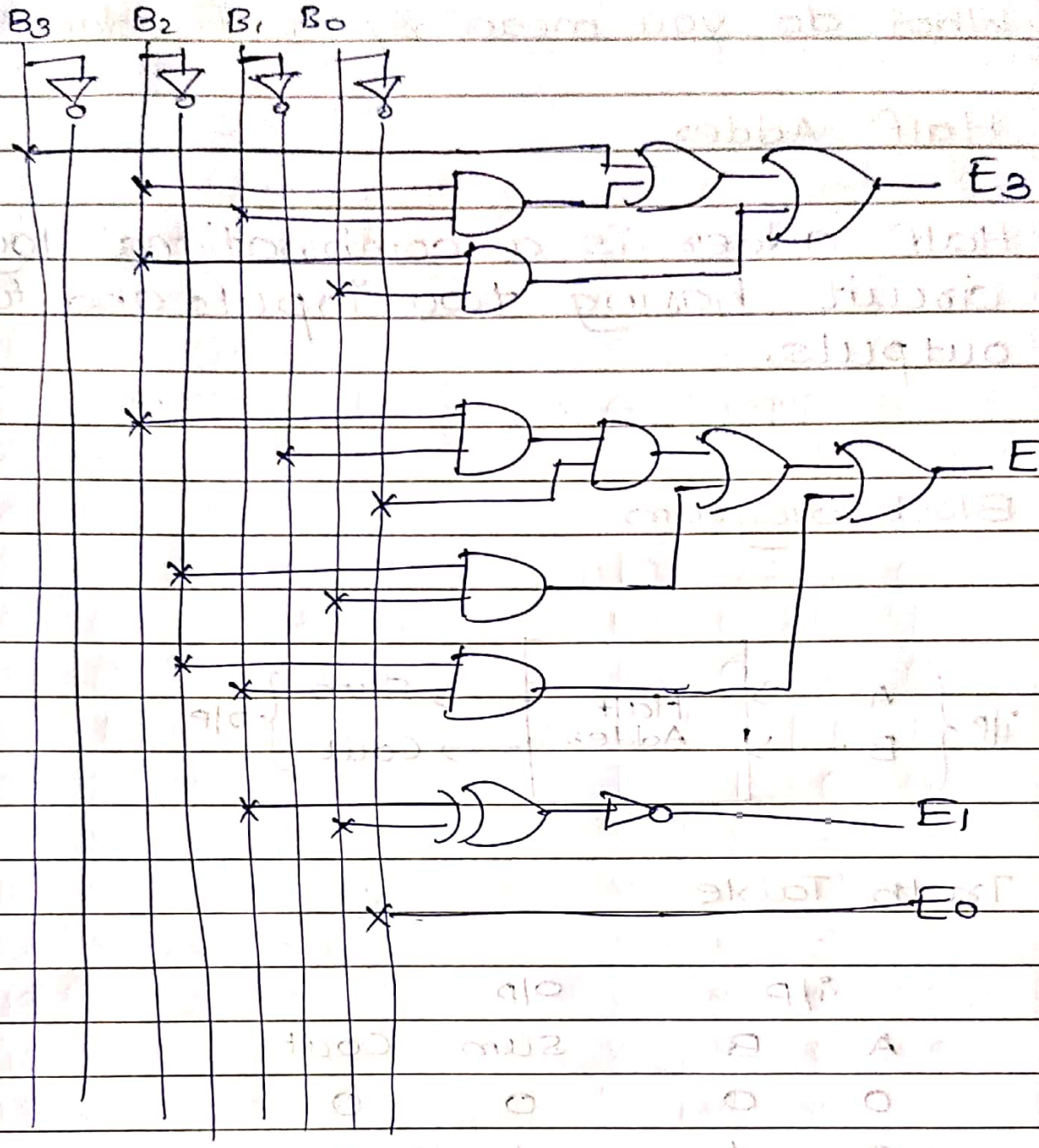
$$E_1 = \bar{B_1}\bar{B_0} + B_1B_0$$
$$= \overline{B_1 \oplus B_0}$$
$$= B_1 \odot B_0$$

K-Map for E_0



$$E_0 = \bar{B_0}$$

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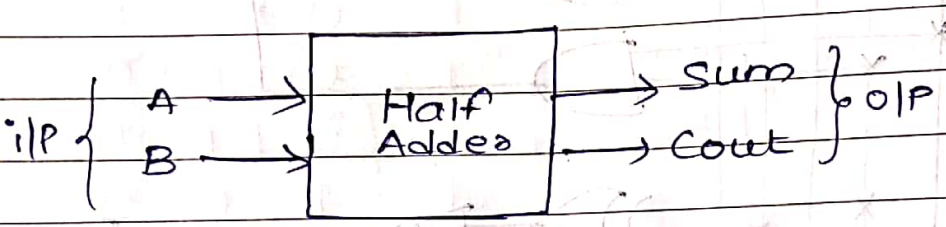
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What do you mean by half adder?

Half Adder

Half adder is a combinational logic circuit having two inputs and two outputs.

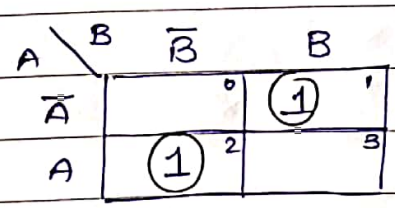
Block diagram



Truth Table

i/p		o/p	
A	B	Sum	Cout
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

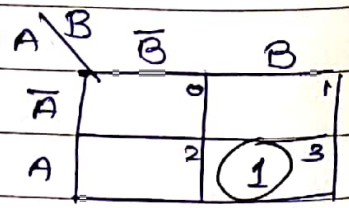
Kmap for sum



$Sum = \bar{A}B + A\bar{B}$

$= A \oplus B$

K-Map for carry

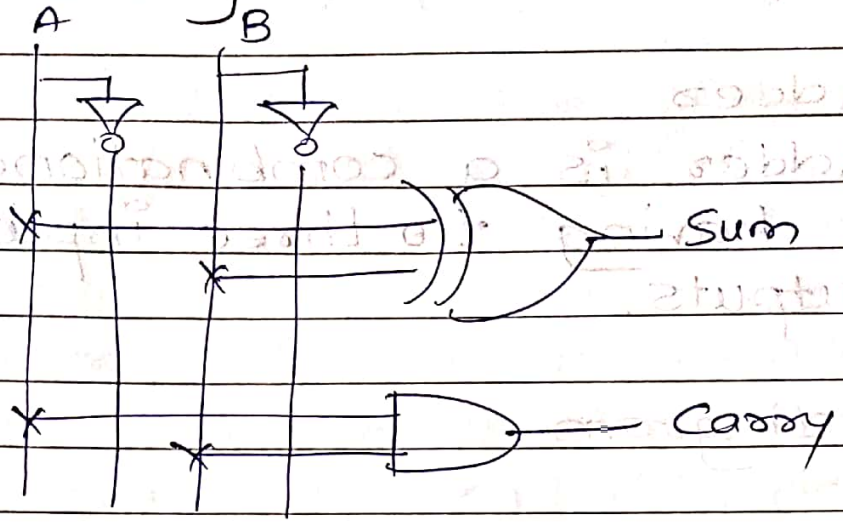


$Carry = AB$

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. logic diagram



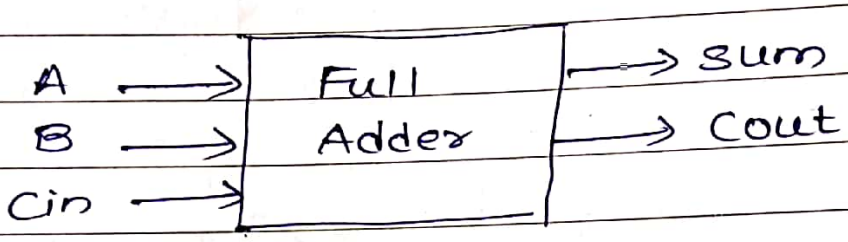
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What do you mean by full Adder

Full Adder

Full Adder is a combinational logic circuit having ~~two~~ three inputs and two outputs.

Block diagram



Truth Table

I/P			O/P	
A	B	Cin	S	Cout
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

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K-Map for Sum

A \ BCin	$\bar{B}\bar{C}in$	$\bar{B}Cin$	$BCin$	$B\bar{C}in$
$\bar{A}$	0	(1) 1	3	(1) 2
A	(1) 4	5	(1) 7	6

$$Sum = \bar{A}\bar{B}Cin + \bar{A}B\bar{C}in + A\bar{B}\bar{C}in + ABCin$$
$$= \bar{A}(\bar{B}Cin + B\bar{C}in) + A(\bar{B}\bar{C}in + BCin)$$
$$= \bar{A}(B \oplus Cin) + A(\overline{B \oplus Cin})$$
$$= A \oplus B \oplus Cin$$

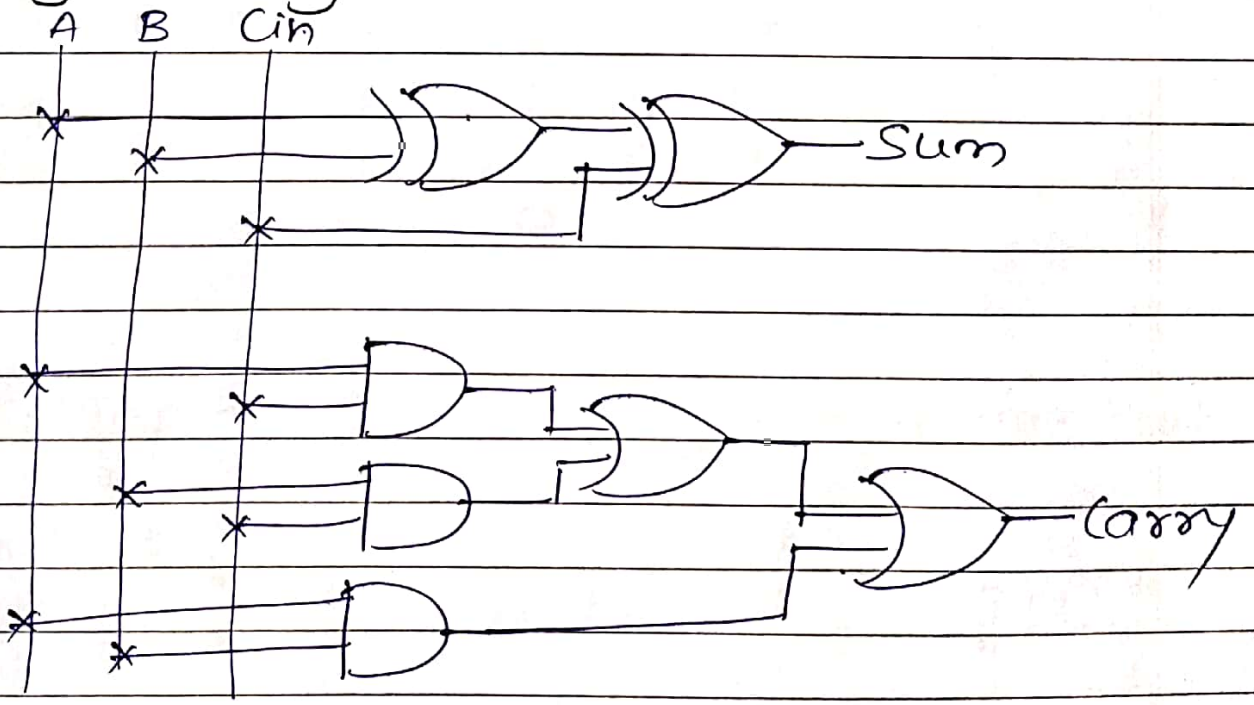
K-Map for Carry

A \ BCin	$\bar{B}\bar{C}in$	$\bar{B}Cin$	$BCin$	$B\bar{C}in$
$\bar{A}$	0	1	(1) 3	2
A	4	(1) 5	(1) 7	(1) 6

① ② ③

$$Carry = ACin + BCin + AB$$

logic diagram



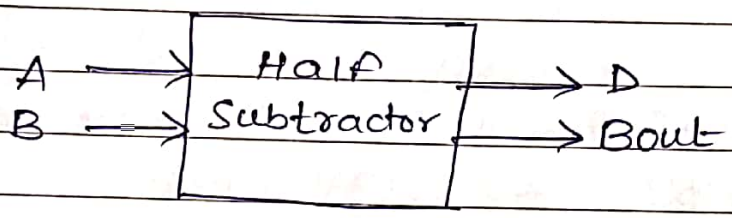
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Describe half subtractor with the help of circuit diagram

Half Subtractor

Half subtractor is a combinational logic circuit having two input and two output.

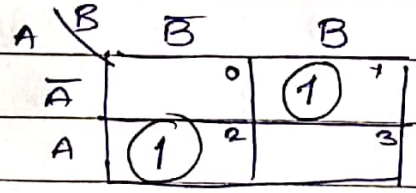
Block diagram



Truth Table

i/p		o/p	
A	B	D	Bout
0	0	0	0
0	1	1	1
1	0	1	0
1	1	0	0

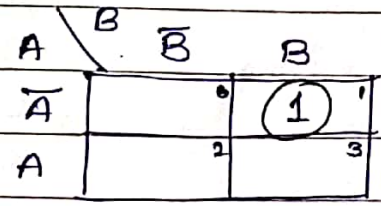
K-Map for D



$D = \bar{A}B + A\bar{B}$

$= A \oplus B$

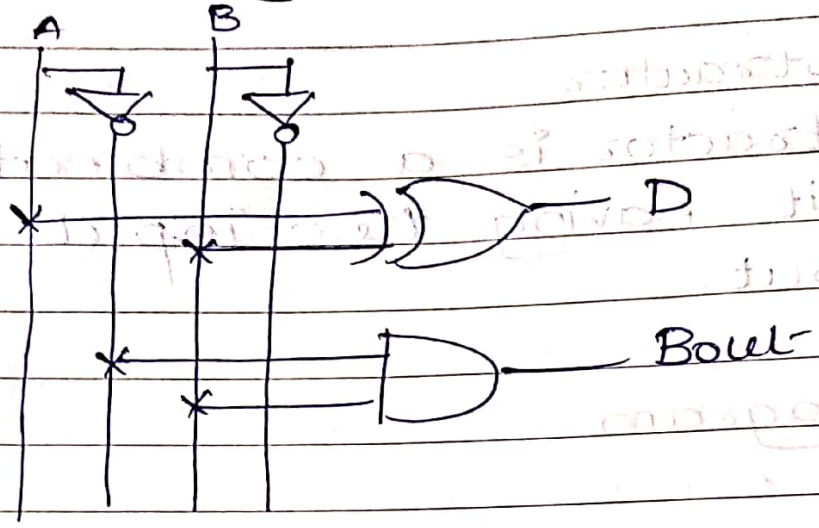
K-Map for Bout



$Bout = \bar{A}B$

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logic diagram



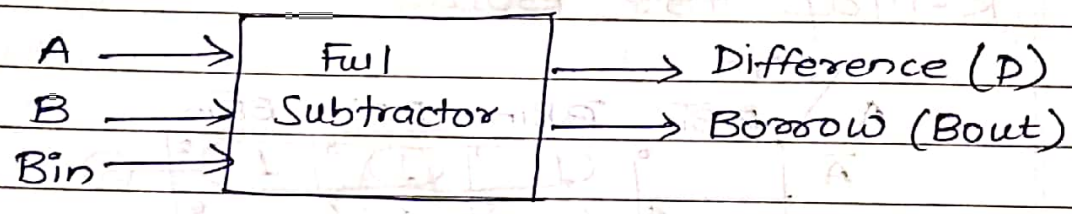
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Draw truth table and logic diagram of full subtractor.

Full Subtractor

full subtractor is a combinational logic circuit with three inputs and two outputs.

Block diagram

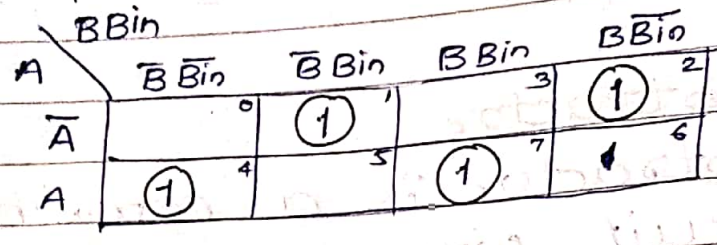


Truth Table

	I/P			O/P	
	A	B	Bin	D	Bout
0	0	0	0	0	0
1	0	0	1	1	1
2	0	1	0	1	1
3	0	1	1	0	1
4	1	0	0	1	0
5	1	0	1	0	0
6	1	1	0	0	0
7	1	1	1	1	1

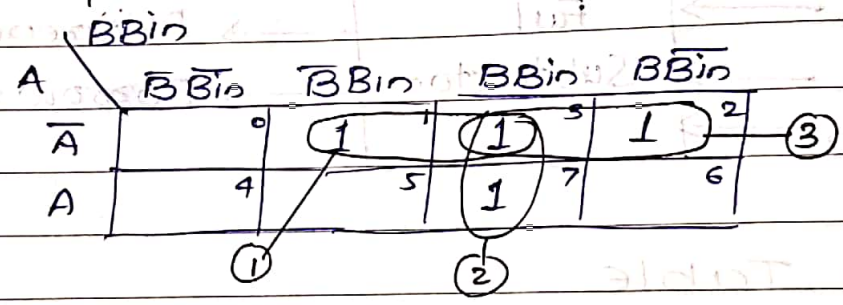
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K-Map for Difference



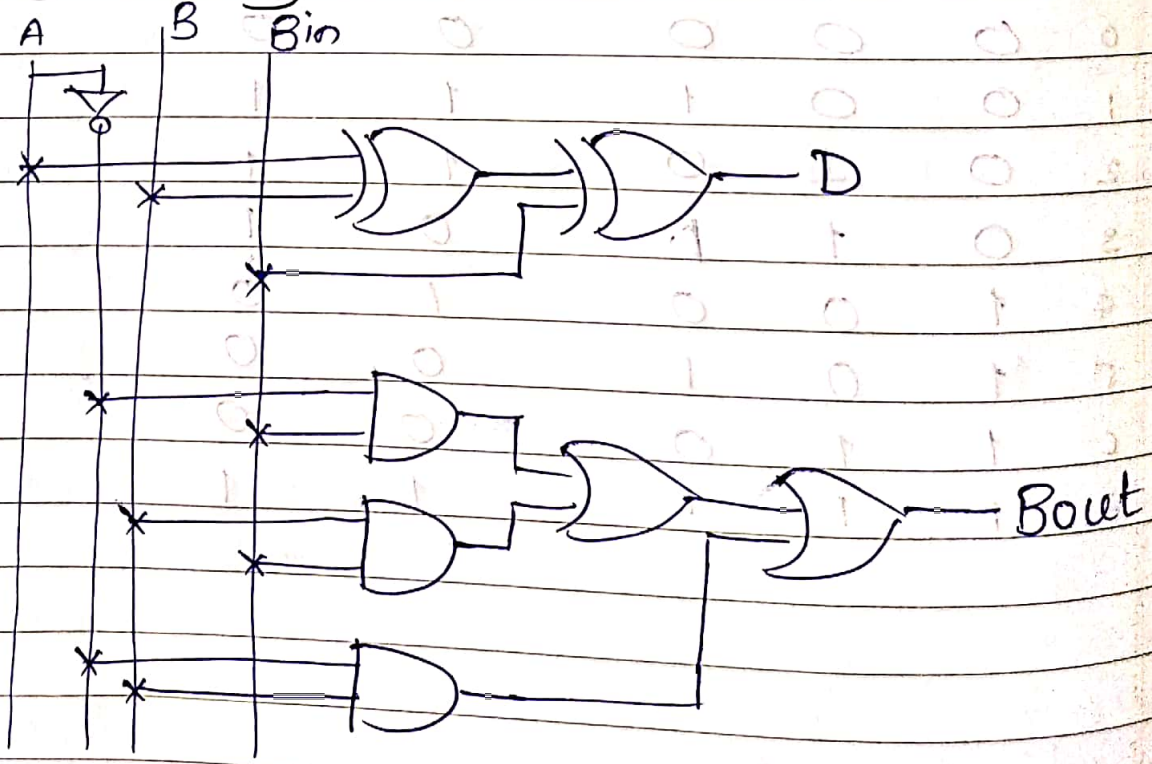
$$D = \bar{A}\bar{B}Bin + \bar{A}B\bar{Bin} + A\bar{B}\cdot\bar{Bin} + ABBin$$
$$= \bar{A}(\bar{B}Bin + B\bar{Bin}) + A(\bar{B}\bar{Bin} + BBin)$$
$$= \bar{A}(B \oplus Bin) + A(\overline{B \oplus Bin})$$
$$= A \oplus B \oplus Bin$$

K-Map for Bout



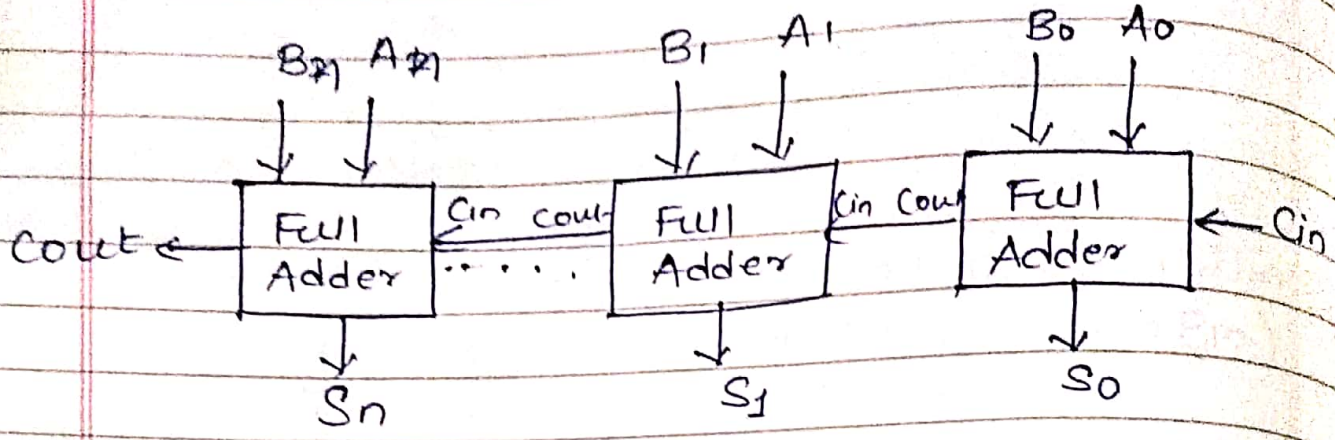
$$Bout = \bar{A}Bin + BBin + \bar{A}B$$

logic diagram



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N-Bit Parallel Adder



An n-bit parallel adder is an arithmetic circuit that adds two binary numbers and generates an arithmetic sum.

The Cout of each full adder is connected to Cin of next full Adder.

Advantages:

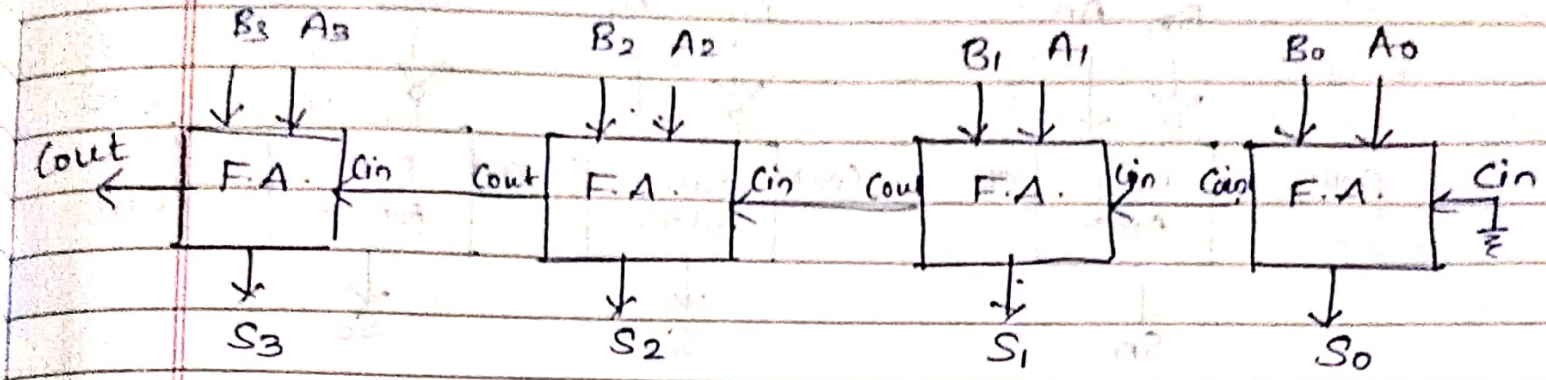
1. Fast processing
2. less time is needed for processing
3. Output available in parallel form
4. Parallel adders are less costly.

Disadvantages:

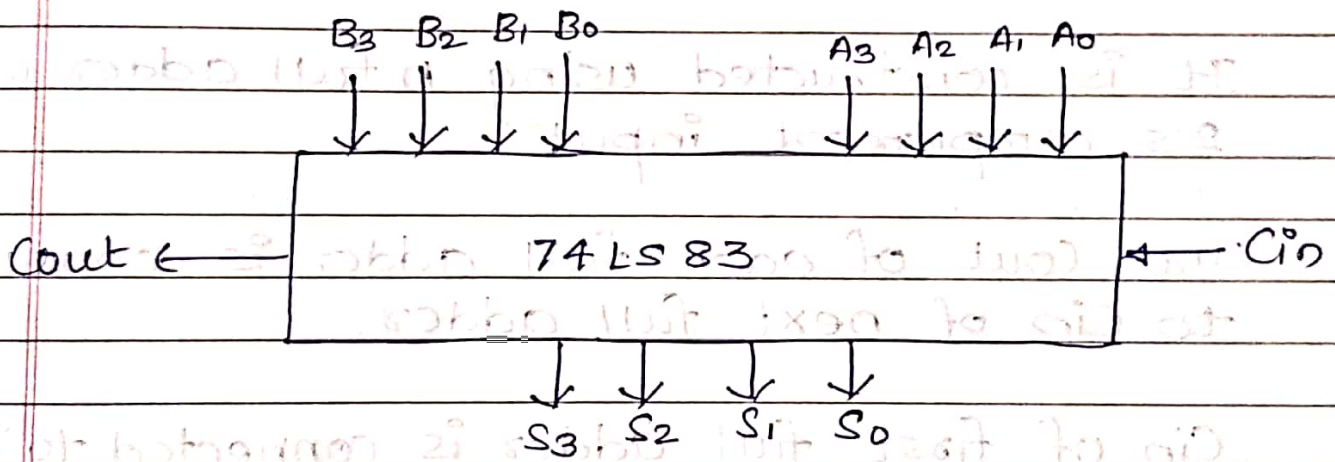
1. If number of bits increases the circuit complexity increases.
2. Every adder has to wait for the carry that is to be generated from previous adder.

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4- bit parallel Adder

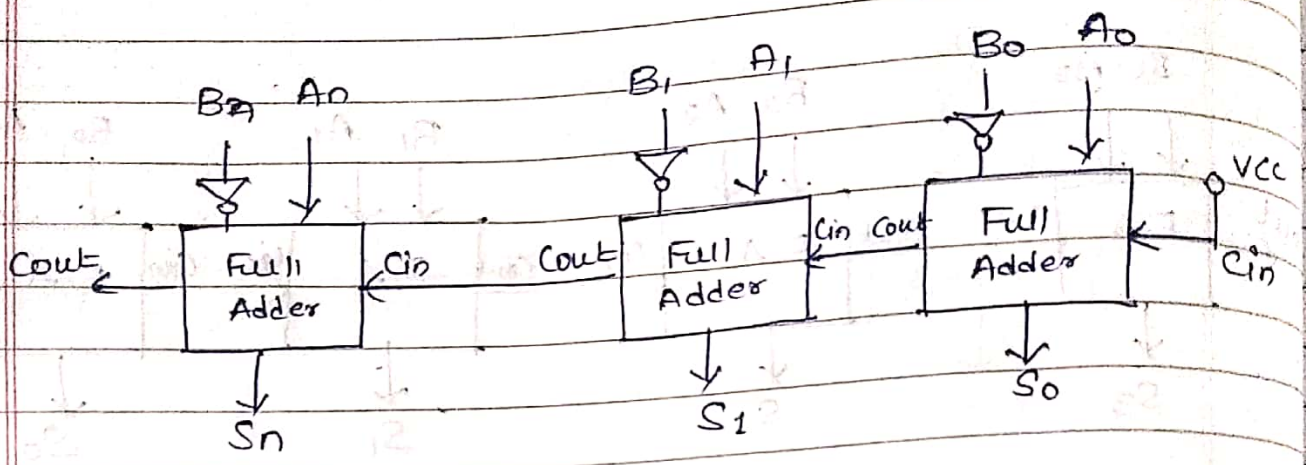


4- bit parallel Adder using IC 7483



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N - Bit Parallel Subtractor



An n bit parallel subtractor is an arithmetic circuit that subtracts binary number and generates arithmetic difference.

It is constructed using n full adder with 2's complement input.

The Cout of each full adder is connected to Cin of next full adder.

Cin of first full adder is connected to Vcc.

Advantages

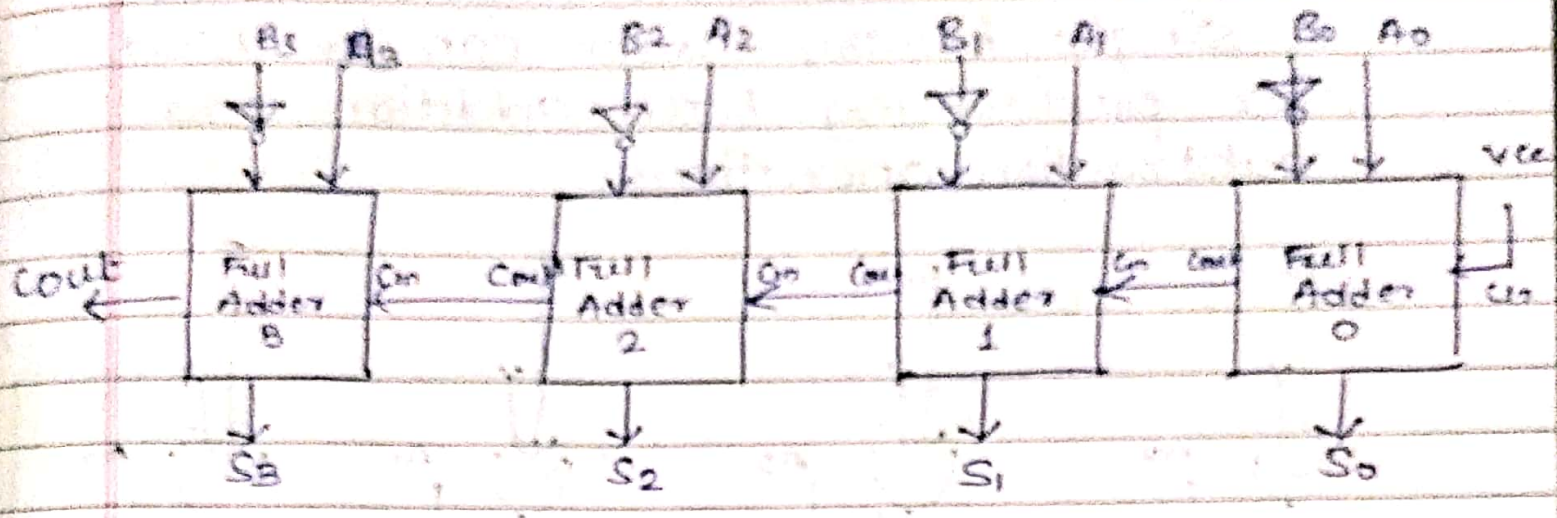
same as n-bit full Adder

Disadvantages

same as n-bit full Adder

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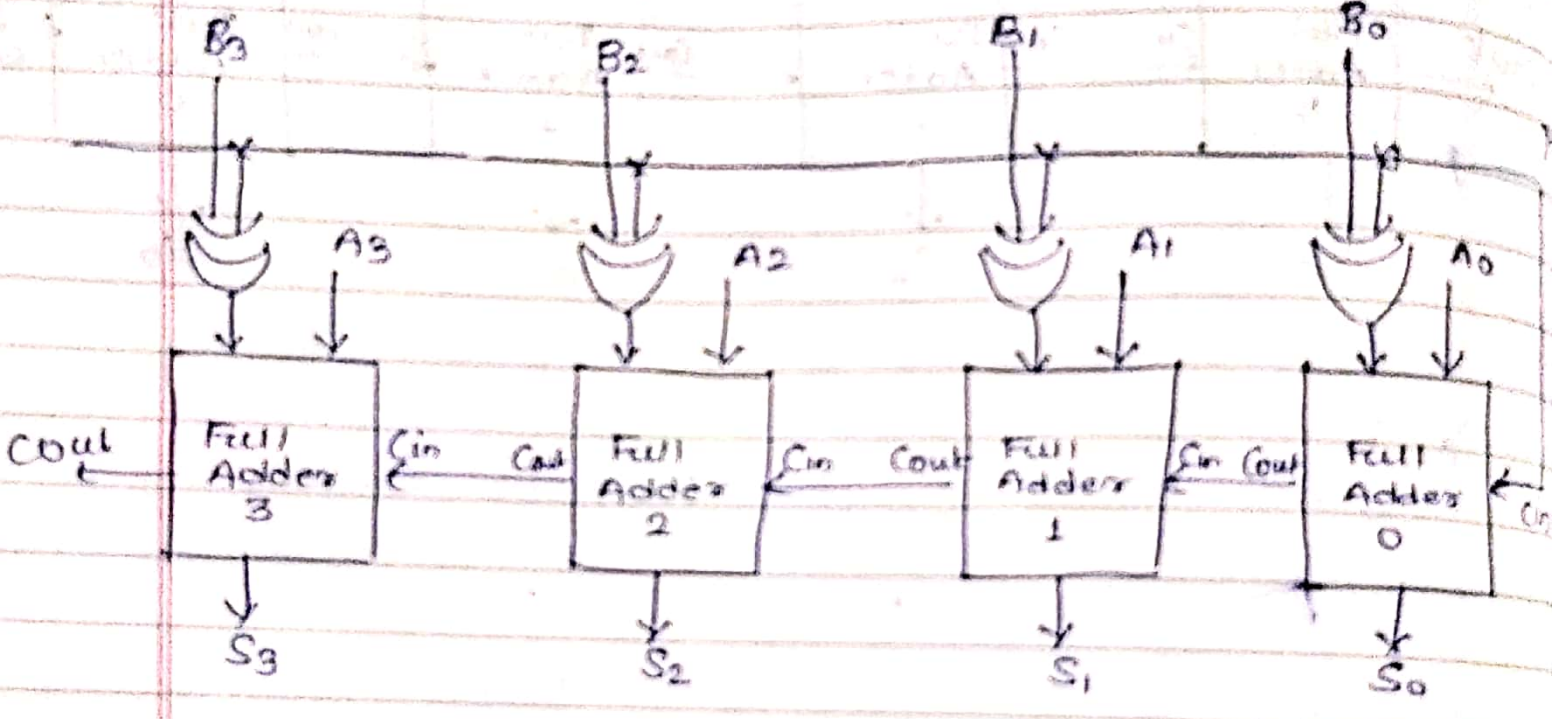
4 bit parallel substractor



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Binary Parallel Adder/Subtractor

A single binary adder can be used for performing both addition and subtraction operations.



M = 0 Circuit performs addition operation

M = 1 Circuit performs subtraction operation

The Ex-OR gate consists of two inputs, one input connected to B input and other to M control line

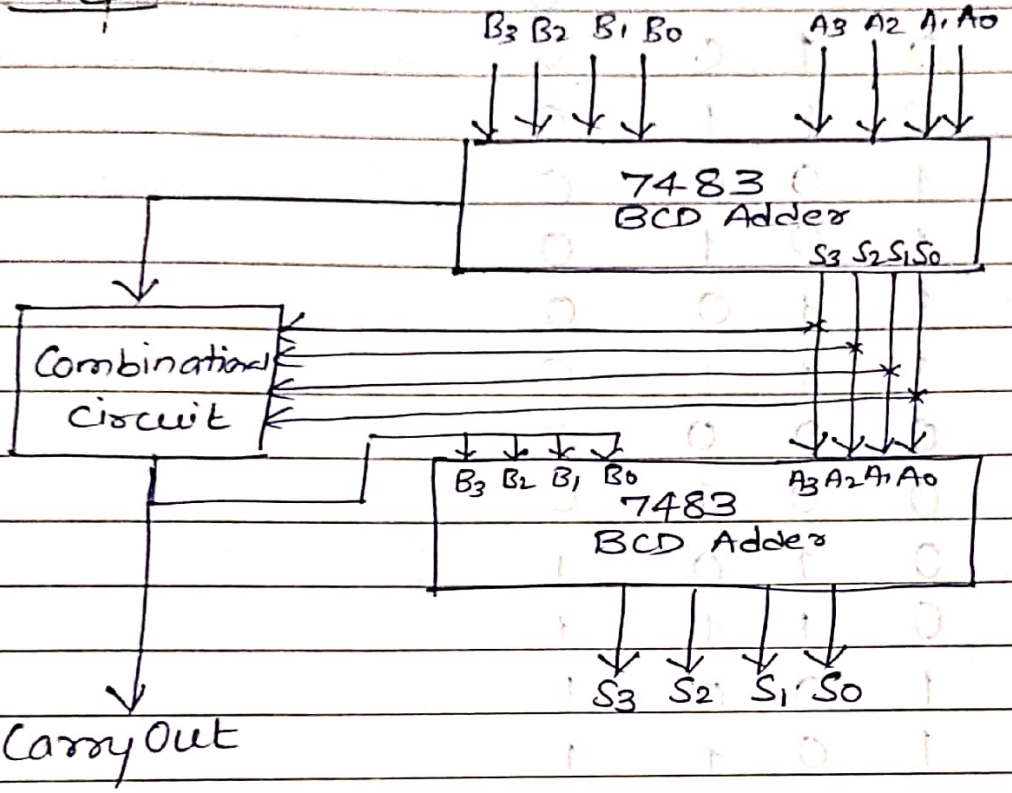
When M=0, B Ex-OR of 0 will produce B
When M=1, B Ex-OR of 1 will produce $\bar{B}$

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Design one digit BCD adder using IC 7483

Design 4 bit BCD adder

Step 1 :



Step 2 Truth table for sum combinational circuit

If the sum is valid BCD then O/P = 0

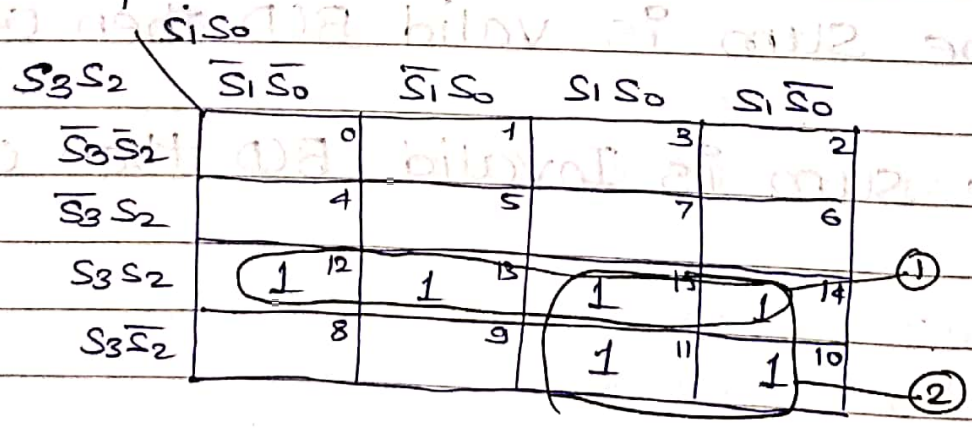
If the sum is Invalid BCD then O/P = 1

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i/p

	S_3	S_2	S_1	S_0	Y
0	0	0	0	0	0
1	0	0	0	1	0
2	0	0	1	0	0
3	0	0	1	1	0
4	0	1	0	0	0
5	0	1	0	1	0
6	0	1	1	0	0
7	0	1	1	1	0
8	1	0	0	0	0
9	1	0	0	1	0
10	1	0	1	0	1
11	1	0	1	1	1
12	1	1	0	0	1
13	1	1	0	1	1
14	1	1	1	0	1
15	1	1	1	1	1

Kmap for Y



$$Y = S_3S_2 + S_3S_1$$

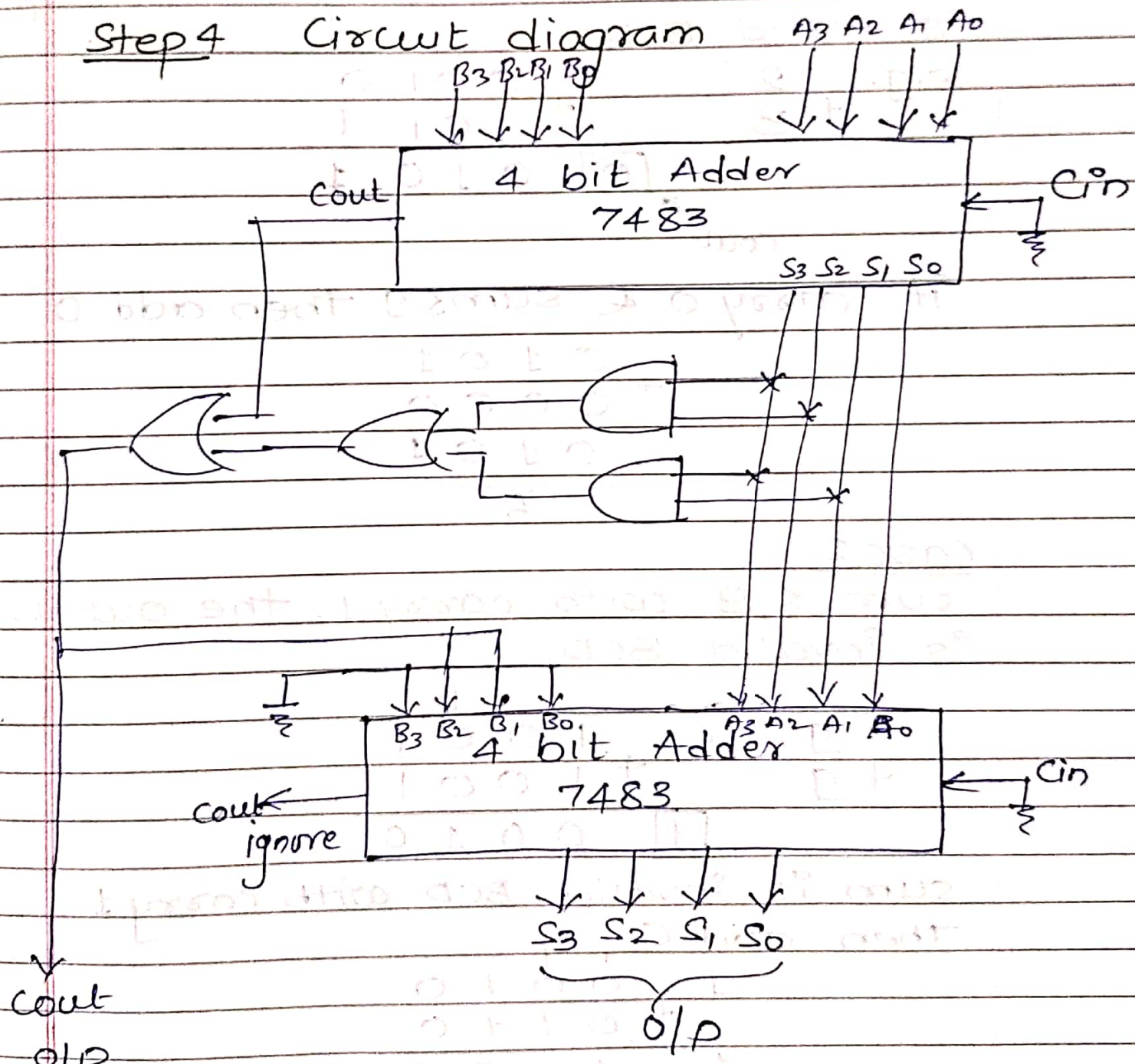
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Step 3

The output is combination circuit of sum o/p and Cout.
so we add Cout of first IC in C combinational circuit.

$\therefore Y = S_3S_2 + S_3S_1 + Cout$

Step 4 Circuit diagram



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Design 4 bit BCD Adder

The two BCD number A and B along with input carry Cin are added in the first 4 bit binary adder to generate BCD sum.

Case 1

sum is ≤ 9 with carry 0, the output is valid BCD

e.g. $2 + 3$

```
    1
  0 0 1 0
+ 0 0 1 1
---------
[0] 0 1 0 1
```

carry

If carry 0 & sum ≤ 9 then add 0

```
  0 1 0 1
+ 0 0 0 0
---------
  0 1 0 1
```

5

Case 2

sum ≤ 9 with carry 1, the output is invalid BCD.

```
    1
  1 0 0 1
+ 1 0 0 1
---------
[1] 0 0 1 0
```

sum is invalid BCD with carry 1

Then add 6

```
  1 1
1 0 0 1 0
+ 0 1 1 0
---------
1 1 0 0 0
```

1 8

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Case 3

Sum > 9 with carry 0 is invalid BCD

$$\begin{array}{r} 8 \\ +5 \end{array} \qquad \begin{array}{r} 1000 \\ +\ 0101 \\ \hline \boxed{0}\ 1101 \end{array}$$

Sum > 9 is invalid BCD then add 6

$$\begin{array}{r} 1 \\ 1101 \\ +\ 0110 \\ \hline 1\ 0011 \end{array}$$

$$1 \qquad 3$$

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