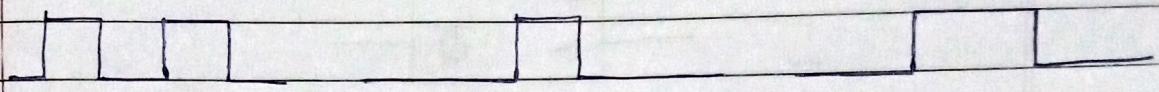
Unit - IV

Flip Flops

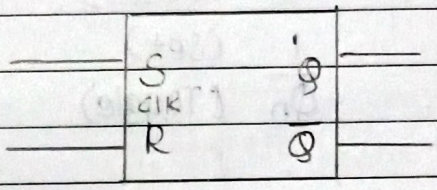
Abstable	Mimostable	Bistable
Both are unstable	1 state stable 1 state unstable	Both are stable.



- Flipflop is Bistable.

* **S-R Flipflop**

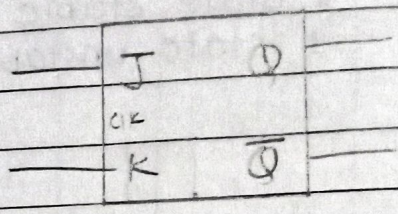
Present state ⇒ Q_n
Next state ⇒ Q_{n+1}



Truth table

S	R	Q_{n+1}	
0	0	Q_n	(No change)
0	1	0	(Reset)
1	0	1	(Set)
1	1	?	(forbidden)

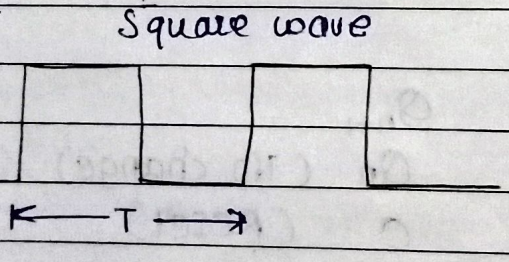
* J-K Flipflop



Truth table

J	K	Q_{n+1}	
0	0	Q_n	(No change)
0	1	0	(Reset)
1	0	1	(Set)
1	1	$\overline{Q_n}$	(Toggle)

* Clock

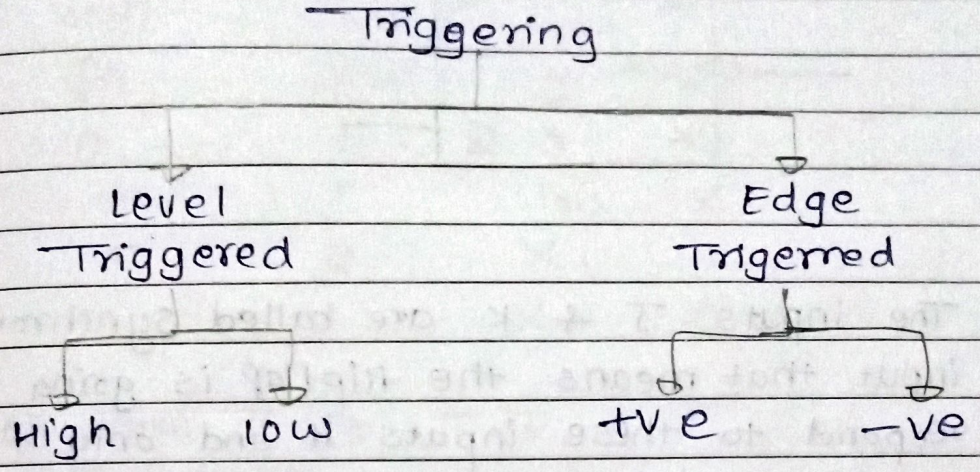


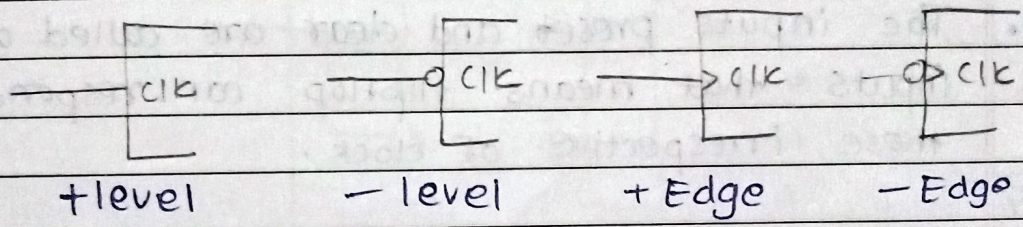
Period 's'

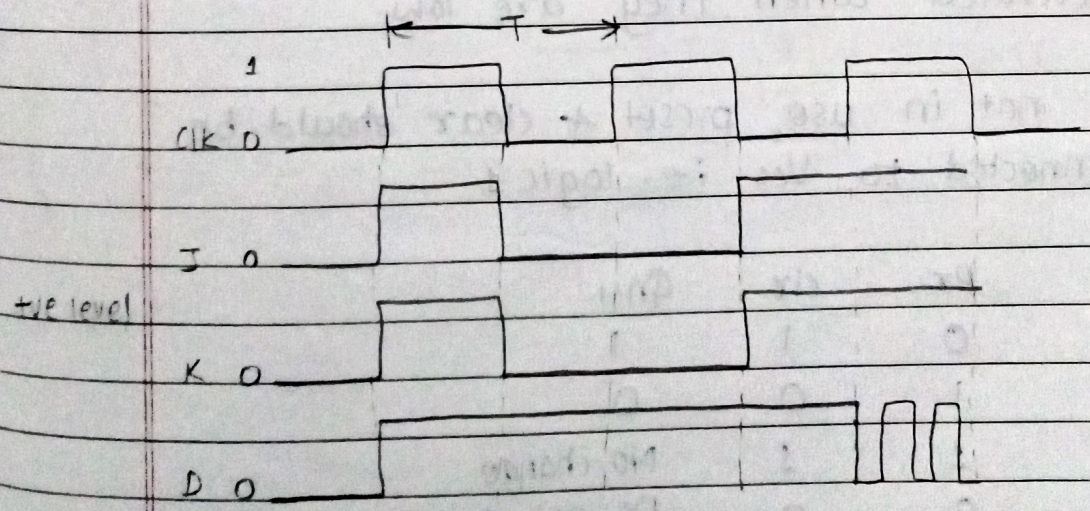
Frequency $f = \frac{1}{T}$ cycles/s = Hz

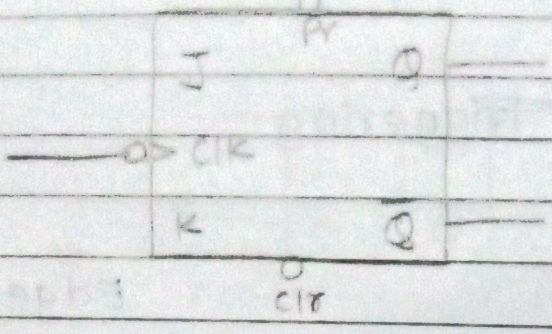
Date
Page

Triggering









- The inputs J & K are called synchronous input that means the flipflop is going to respond to these inputs if and only if the clock is present.

- The inputs preset and clear are called asynchronous inputs. that means flipflop can respond to these, irrespective of clock.

- Preset and clear are active low that means activated when they are low.

- If not in use, preset & clear should be connected to Vcc i.e. logic 1.

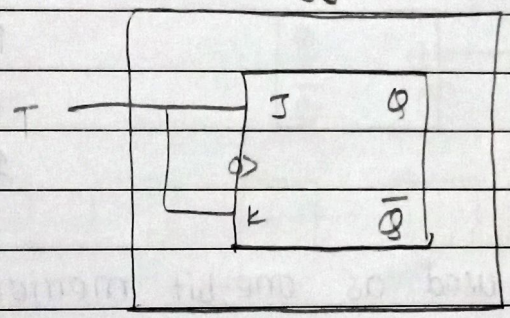
Pr	clr	Q_{n+1}
0	1	1
1	0	0
1	1	No change
0	0	Do not Apply

Date
Page

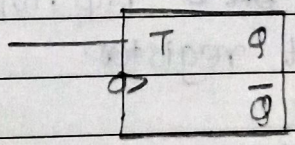
- Excitation table

Present state	Next state	I/p	
Q_n	Q_{n+1}	J	K
0	0	0	X
0	1	1	X
1	0	X	1
1	1	X	0

* Conversion of J-K T-FF into T-flipflop (Toggle)



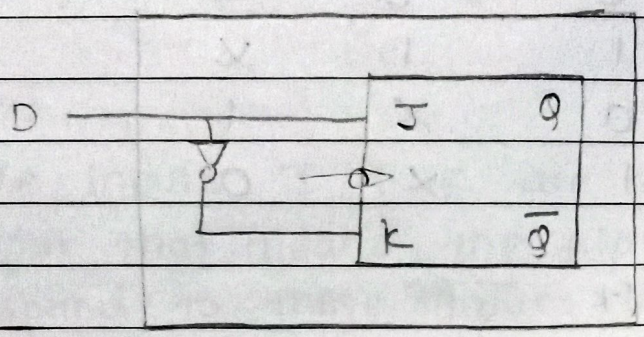
J	K	Q_{n+1}
0	0	Q_n
0	1	0
1	0	1
1	1	$\overline{Q_n}$

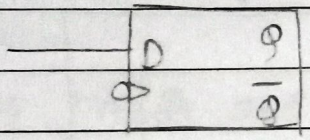


T	Q_{n+1}	
0	Q_n	No change
1	$\overline{Q_n}$	

* Conversion of J-K flipflop into D-flipflop

D-FF
(Delay)



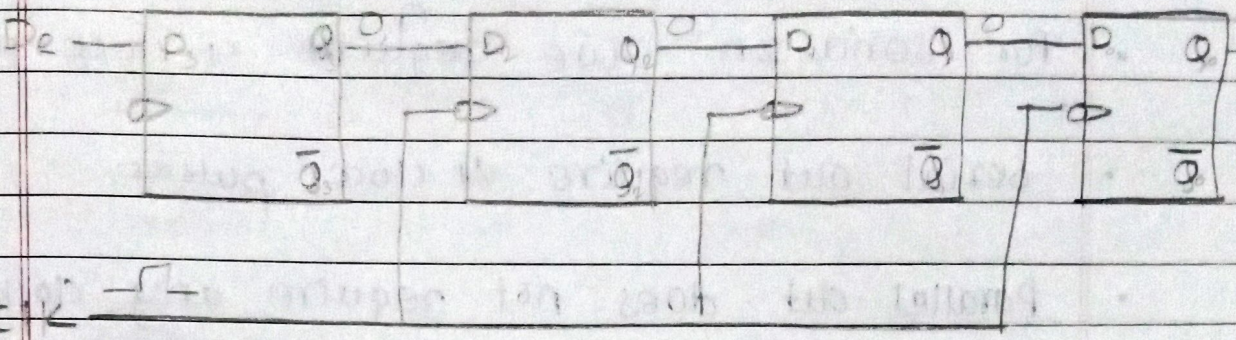


D	Q_{n+1}
0	0
1	1

- D flipflop is used as one-bit memory cell. If we want to make 8-bit storage element we require 8 D flip-flops. This arrangement is called 8-bit register.

* 4-bit right shift register (using D flipflop)

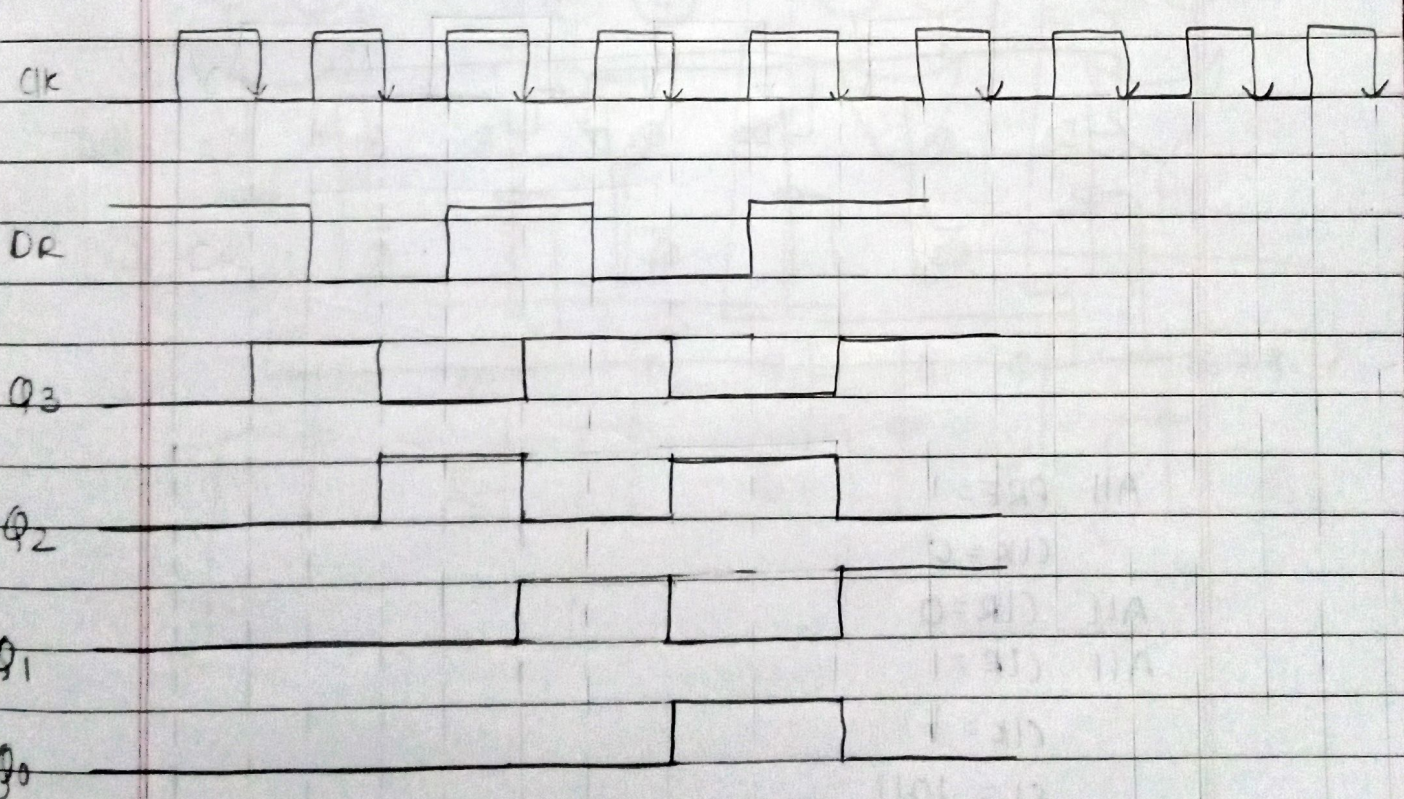
* 4-bit right shif register (using D flipflop)



CLOCK = 0
ALLCLEAR = 0

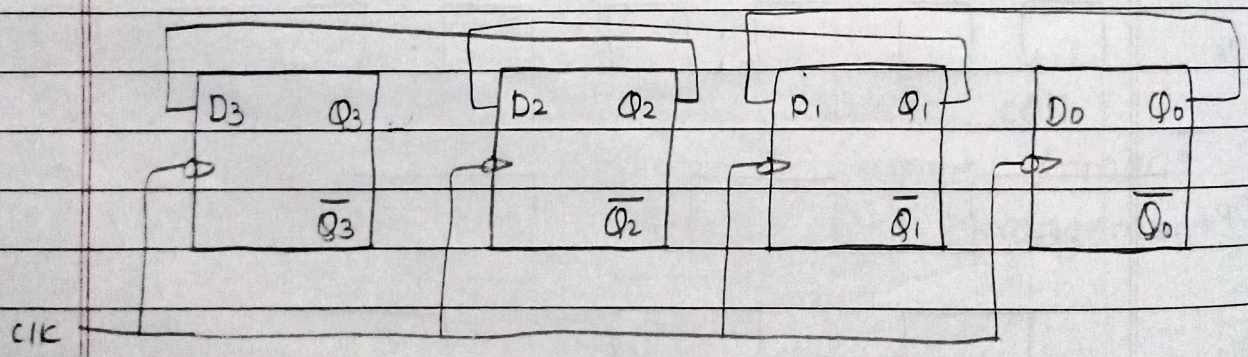
ALLCLEAR = 1
CLOCK = 1 DR = 1

▶ Waveform



- This circuit offers SISO (serial in serial out) and SIPO (serial In Parallel Out)
- For serial In, we require 4 clock pulses.
- Serial out require 4 clock pulses.
- Parallel out does not require any clock pulse

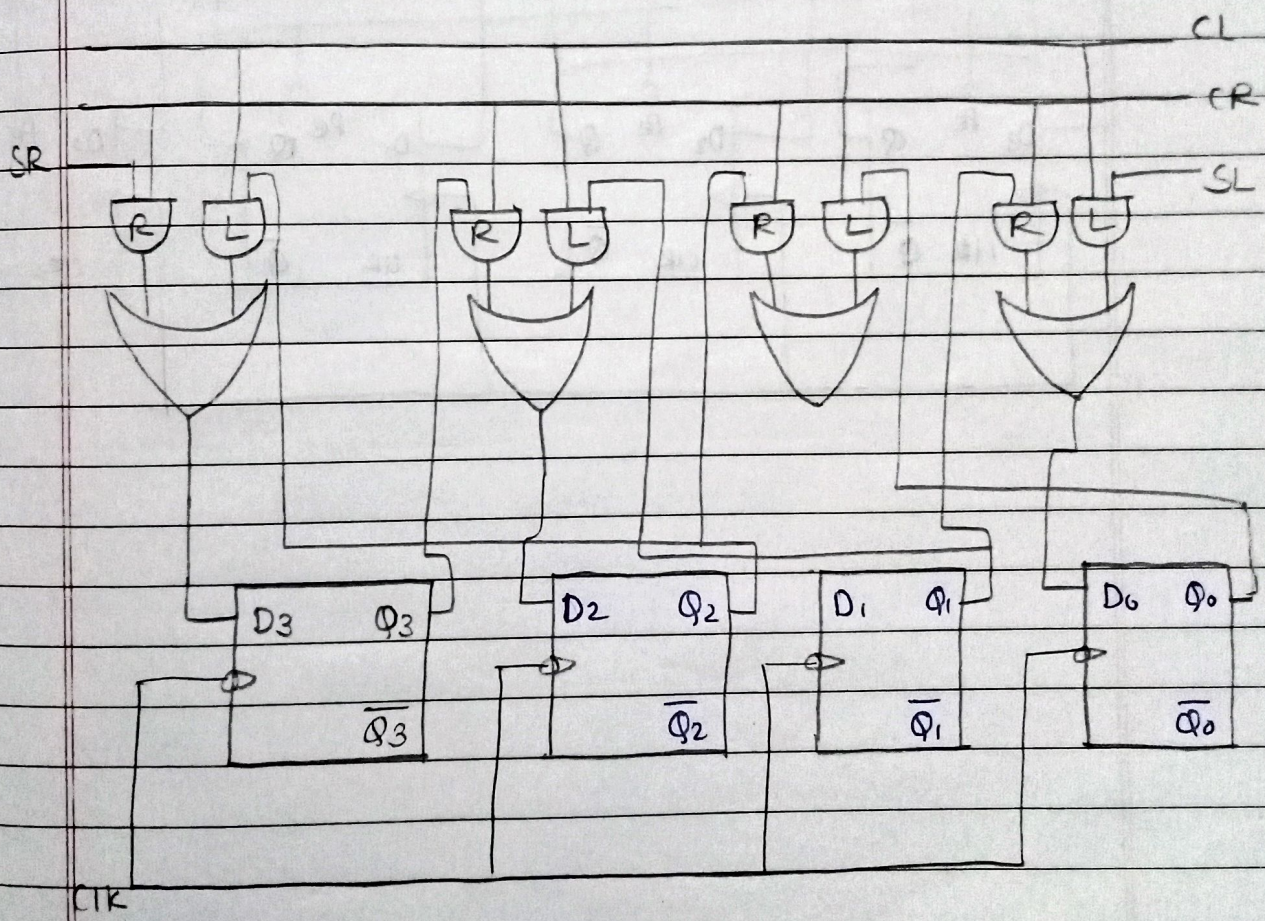
* 4 bit left shift resistor
* L-S Flipflop

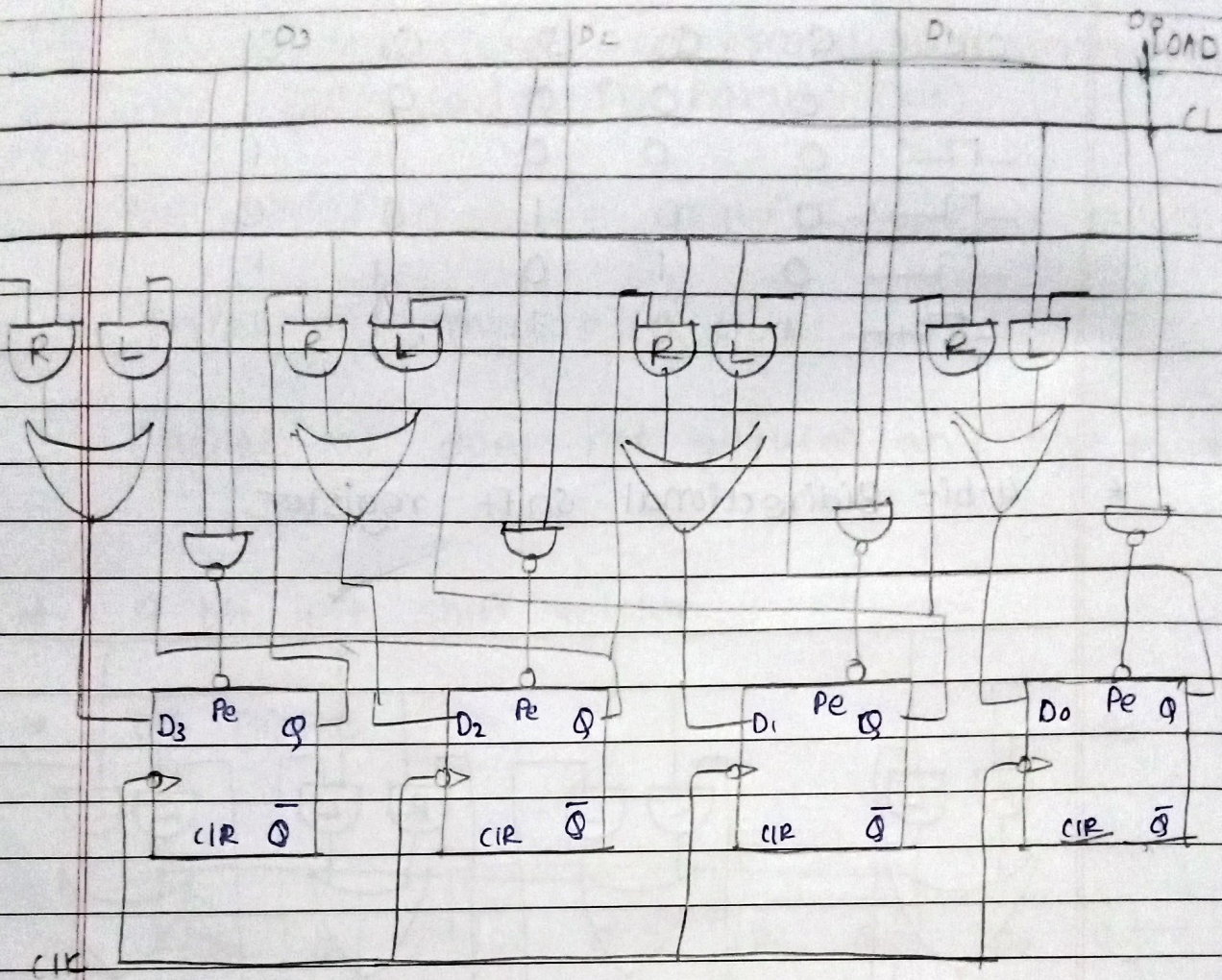


All PRE = 1
CLK = 0
All CLR = 0
All CLR = 1
CLK = 1
SL = 1011

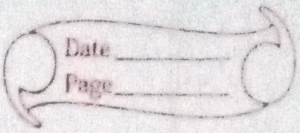
CLK	Q_3	Q_2	Q_1	Q_0	SL
	0	0	0	0	
⎍	0	0	0	1	1
⎍	0	0	1	0	0
⎍	0	1	0	1	1
⎍	1	0	1	1	1

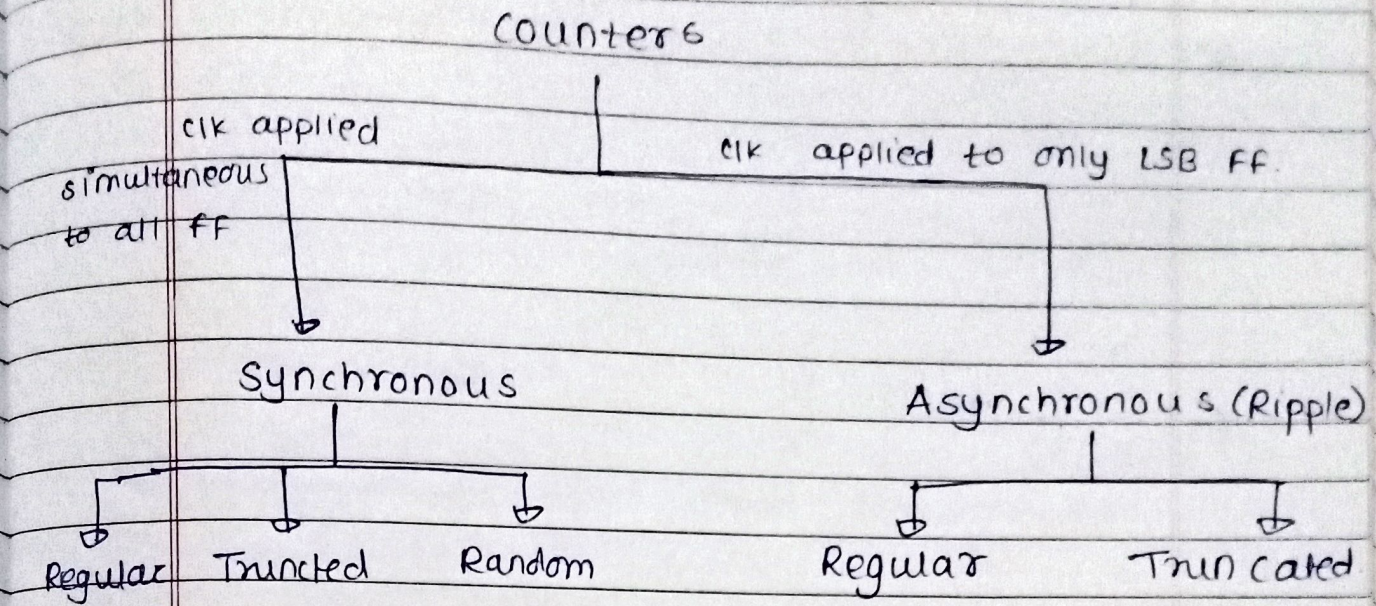
* 4-bit Bidirectional shift register




D3
D2
D1
D0
LOAD
CL
CR
R
L
D3 Pe Q
D2 Pe Q
D1 Pe Q
D0 Pe Q
CLR Q̄
CLR Q̄
CLR Q̄
CLR Q̄
CLK

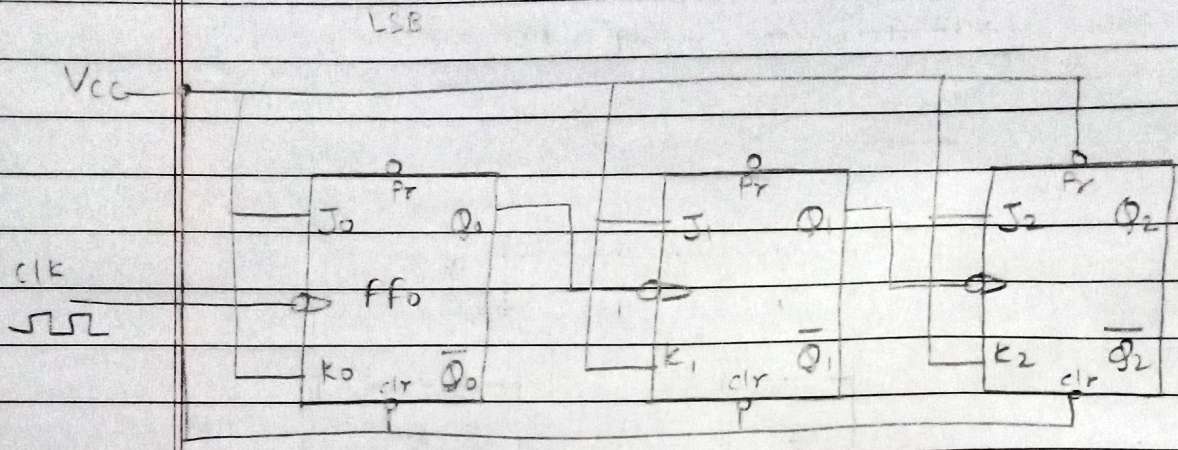
Unit 5


Date
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Counters
clk applied simultaneous to all FF
clk applied to only LSB FF
Synchronous
Asynchronous (Ripple)
Regular
Truncted
Random
Regular
Truncated

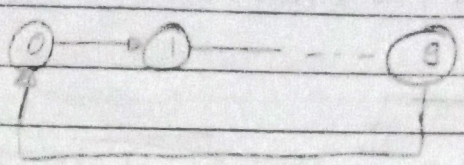
Date
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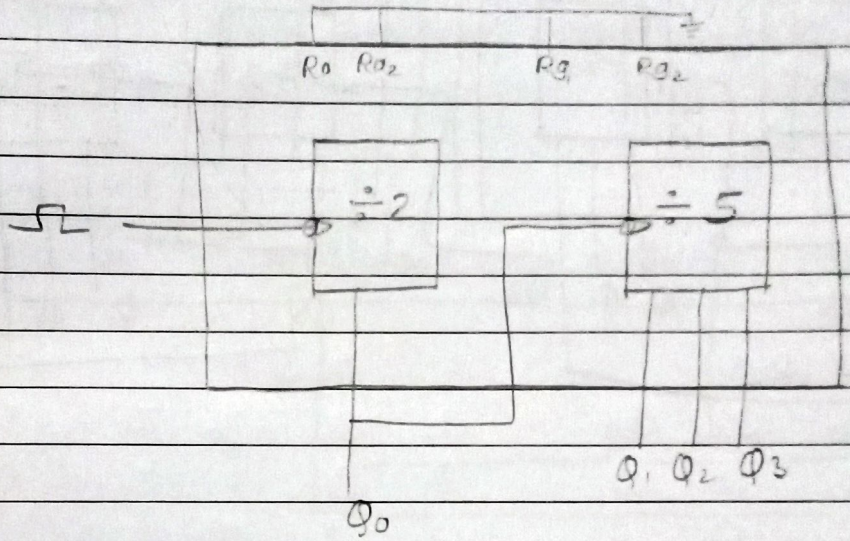
* 3-bit Asynchronous (Ripple) counter using JK flipflop



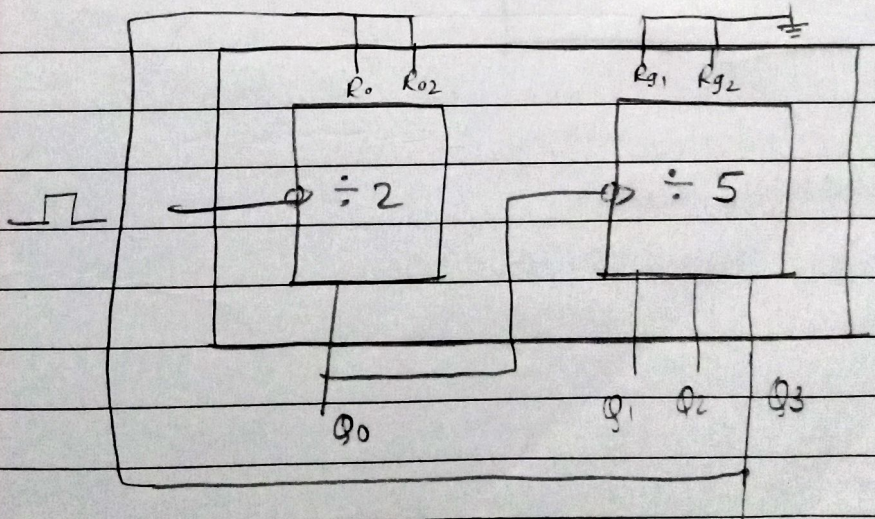
Q_n P.S.			Q_{n+1} N.S		
Q_2	Q_1	Q_0	Q_2	Q_1	Q_0
0	0	0	0	0	1
0	0	1	0	1	0
0	1	0	0	1	1
0	1	1	1	0	0
1	0	0	1	0	1
1	0	1	1	1	0
1	1	0	1	1	1
1	1	1	0	0	0

* Decade /BCD/ MOD-10 Ripple counter (IC 7490)



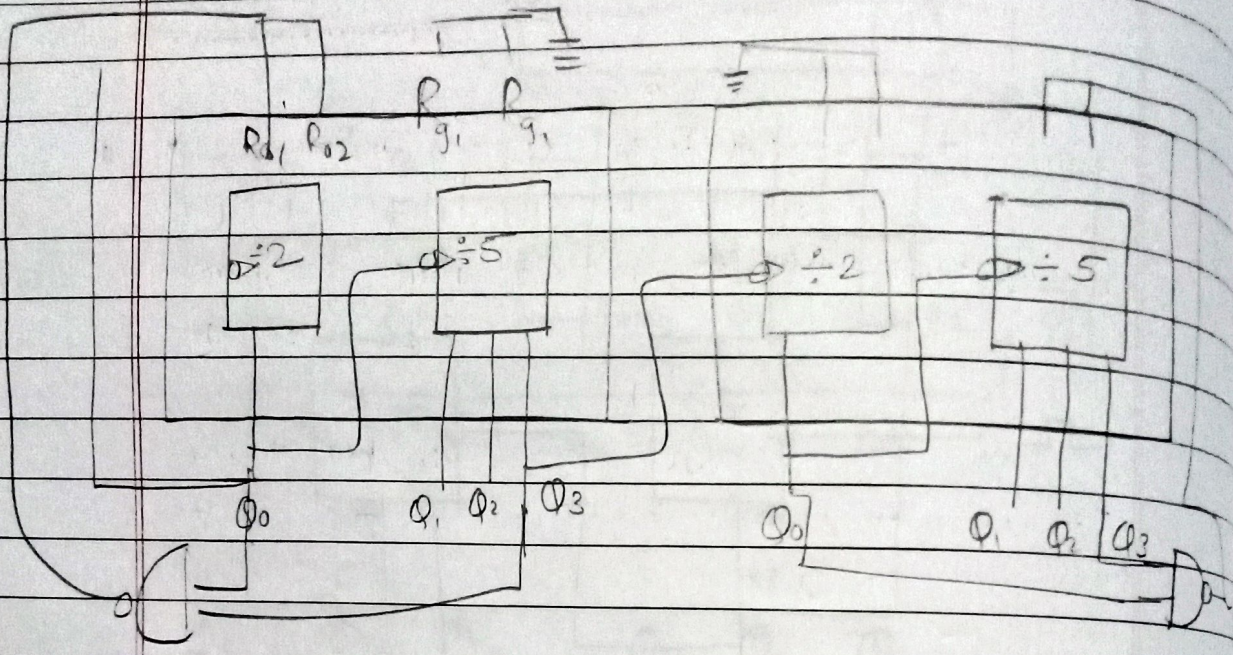


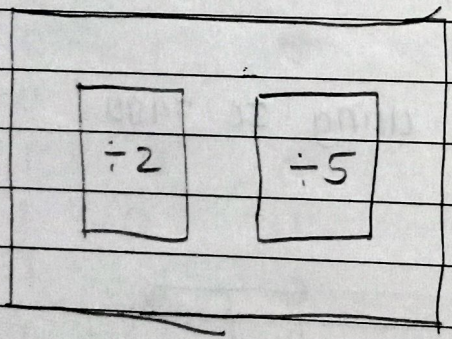
Q. Design Mod 8 counter using IC 7490



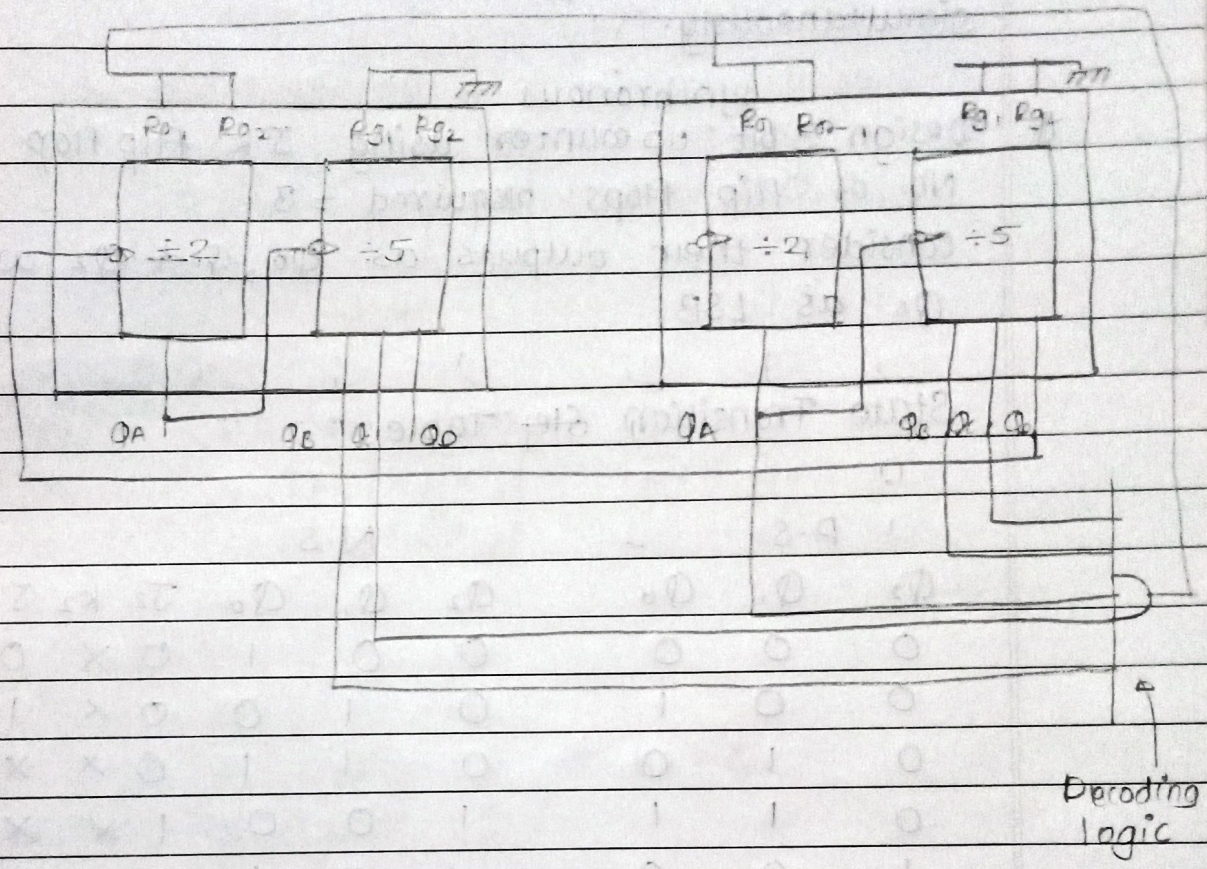
Q.1] Design MOD-100 counter using Ripple counter

Q.2] Design MOD-67 counter using Ripple counter





We have to decode the state 67
i.e. 0110 0111 in BCD.



* Q. Design of synchronous counters

Clock pulses are applied to all the flip-flops simultaneously.

synchronous

Q. Design 3-bit up counter using J-K flip flop

No. of flip flops required = 3

Consider their outputs as Q_0, Q_1 & Q_2 with Q_0 as LSB

State Transition ~~Ste~~ Table:

P.S.			N.S								
Q_2	Q_1	Q_0	Q_2	Q_1	Q_0	J_2	K_2	J_1	K_1	J_0	K_0
0	0	0	0	0	1	0	X	0	X	1	X
0	0	1	0	1	0	0	X	1	X	X	1
0	1	0	0	1	1	0	X	X	0	1	X
0	1	1	1	0	0	1	X	X	1	X	1
1	0	0	1	0	1	X	0	0	X	1	X
1	0	1	1	1	0	X	0	1	X	X	1
1	1	0	1	1	1	X	0	X	0	1	X
1	1	1	0	0	0	X	1	X	1	X	1

Excitation Table

Q_n	Q_{n+1}	J	K
0	0	0	x
0	1	1	x
1	0	x	1
1	1	x	0

Date
Page

J_2:

Q_2 \ Q_1Q_0	00	01	11	10
0	0	1	3	2
1	X 4	X 5	X 7	X 6

$J_2 = Q_1Q_0$

K_2:

Q_2 \ Q_1Q_0	00	01	11	10
0	X 0	X 1	X 3	X 2
1	4	5	1 7	6

$K_2 = Q_1Q_0$

J_1:

Q_2 \ Q_1Q_0	00	01	11	10
0	0	1 1	X 3	X 2
1	4	1 5	X 7	X 6

$J_1 = Q_0$

K_1:

Q_2 \ Q_1Q_0	00	01	11	10
0	X 0	X 1	1 3	2
1	X 4	X 5	1 7	6

$K_1 = Q_0$

J_0:

Q_2 \ Q_1Q_0	00	01	11	10
0	1 0	X 1	X 3	1 2
1	1 4	X 5	X 7	1 6

$J_0 = J_0$

K_0:

Q_2 \ Q_1Q_0	00	01	11	10
0	X 0	1 1	1 3	X 2
1	X 4	1 5	1 7	X 6

$K_0 = K_0$

- All preset & clear connected to Vcc i.e. logic 1.
- Clock is applied simultaneously to all.

Q. Design 3-bit synchronous down counter using J-K flip flop.

No. of flip flops required = 3

Outputs ⟹ Q_0, Q_1 & Q_2 with Q_0 as LSB

State transition table:

P.S.			N.S								
Q_2	Q_1	Q_0	Q_2	Q_1	Q_0	J_2	K_2	J_1	K_1	J_0	K_0
0	0	0	1	1	1	1	x	1	x	1	x
0	0	1	1	1	0	1	x	1	x	x	1
0	1	0	1	0	1	1	x	x	1	1	x
0	1	1	1	0	0	1	x	x	1	x	1
1	0	0	0	1	1	x	1	1	x	1	x
1	0	1	0	1	0	x	1	1	x	x	1
1	1	0	0	0	1	x	1	x	1	1	x
1	1	1	0	0	0	x	1	x	1	x	1

Excitation table:

Q_n	Q_{n+1}	J	K
0	0	0	x
0	1	1	x
1	0	x	1
1	1	x	0

J_2 :

Q_2 \ Q_1Q_0	00	01	11	10
0	1	1	1	1
1	X	X	X	X

$J_2 = J_2$

K_2 :

Q_2 \ Q_1Q_0	00	01	11	10
0	X	X	X	X
1	1	1	1	1

$K_2 = K_2$

J_0	K_0
1	X
X	1
1	X
X	1
1	X
X	1
1	X
X	1

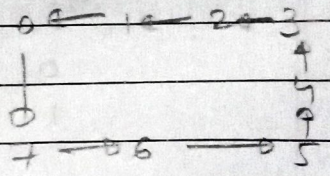
J_1 :

Q_2 \ Q_1Q_0	00	01	11	10
0	0	1	3	2
1	4	5	7	6

- All preset & clear are connected to Vcc i.e. logic 1
- clock is applied simultaneously to all

Q. Design 3-bit synchronous down counter using

State transition table:



P.S.			N.S.								
Q_2	Q_1	Q_0	Q_2	Q_1	Q_0	J_2	K_2	J_1	K_1	J_0	K_0
0	0	0	1	1	1	1	X	1	X	1	X
0	0	1	0	0	0	0	X	0	X	X	1
0	1	0	0	0	1	0	X	X	1	1	X
0	1	1	0	1	0	0	X	X	0	X	1
1	0	0	0	1	1	X	1	1	X	1	X
1	0	1	1	0	0	X	0	0	X	X	1
1	1	0	1	0	1	X	0	X	1	1	X
1	1	1	1	1	0	X	0	X	0	X	1

Excitation Table:

Q_n	Q_{n+1}	J	K
0	0	0	X
0	1	1	X
1	0	X	1
1	1	X	0

J_2:

Q_2 \ Q_1Q_0	00	01	11	10
0	1			
1	X	X	X	X

$J_2 = \bar{Q_1}\bar{Q_0}$

K_2:

Q_2 \ Q_1Q_0	00	01	11	10
0	X	X	X	X
1	1			

$K_2 = \bar{Q_1}\bar{Q_0}$

J_1:

Q_2 \ Q_1Q_0	00	01	11	10
0	1		X	X
1	1		X	X

$J_1 = \bar{Q_0}$

K_1:

Q_2 \ Q_1Q_0	00	01	11	10
0	X	X		1
1	X	X		1

$K_1 = \bar{Q_0}$

J_0:

Q_2 \ Q_1Q_0	00	01	11	10
0	1	X	X	1
1	1	X	X	1

$J_0 = \bar{Q} \cdot J_0$

K_0:

Q_2 \ Q_1Q_0	00	01	11	10
0	X	1	1	X
1	X	1	1	X

$K_0 = k_0$

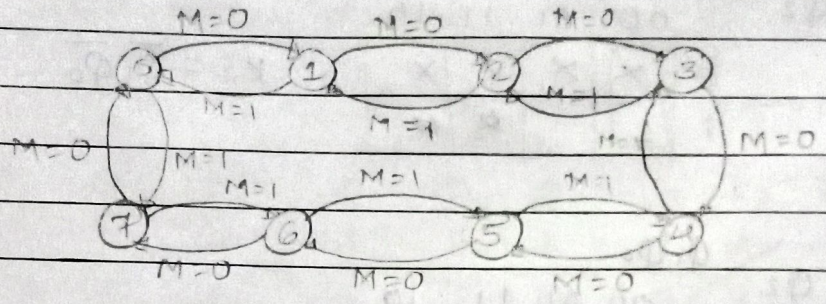
Q. Design 3-bit synchronous up/down counter with mod control M using J-K flipflop

If M=0, count up.

If M=1, count down.

(a) "1":

State diagram:



State Transition step(Table)

	P.S.			N.S.								
M	Q_2	Q_1	Q_0	Q_2	Q_1	Q_0	J_2	K_2	J_1	K_1	J_0	K_0
0	0	0	0	0	0	1	0	X	0	X	1	X
0	0	0	1	0	1	0	0	X	1	X	X	1
0	0	1	0	0	1	1	0	X	X	0	1	X
0	0	1	1	1	0	0	1	X	X	1	X	1
0	1	0	0	1	0	1	X	0	0	X	1	X
0	1	0	1	1	1	0	X	0	1	X	X	1
0	1	1	0	1	1	1	X	0	X	0	1	X
0	1	1	1	0	0	0	X	1	X	1	X	1
1	0	0	0	1	1	1	1	X	1	X	1	X
1	0	0	1	0	0	0	0	X	0	X	X	1
1	0	1	0	0	0	1	0	X	X	1	1	X
1	0	1	1	0	1	0	0	X	X	1	X	1
1	1	0	0	0	1	1	X	0	1	X	1	X
1	1	0	1	1	0	0	X	1	0	X	X	1
1	1	1	0	1	0	1	X	0	X	0	1	X
1	1	1	1	1	1	0	X	0	X	0	X	1

Excitation table:

Q_n	Q_{n+1}	J	K
0	0	0	x
0	1	1	x
1	0	x	1
1	1	x	0

- K-map:

J_2:

MQ_2 \ Q_1Q_0	00	01	11	10
00	0	1	3	2
01	x 4	x 5	x 7	x 6
11	x 12	x 13	x 15	x 14
10	1 8	9	11	10

$J_2 = \bar{M} Q_1 Q_0 + M \bar{Q_1} \bar{Q_0}$

K_2:

MQ_2 \ Q_1Q_0	00	01	11	10
00	x	x	x	x
01	0	0	1	0
11	x	x	0	0
10	x	x	x	x

$K_2 = \bar{M} Q_1 Q_0 + M \bar{Q_1} \bar{Q_0}$

J_1:

MQ_2 \ Q_1Q_0	00	01	11	10
00	0	1 1	x 3	x 2
01	4	1 5	x 7	x 6
11	1 12	13	x 15	x 14
10	1 8	0 9	x 11	x 10

$J_1 = M \bar{Q_0} + \bar{M} Q_0$

K_1:

MQ_2 \ Q_1Q_0	00	01	11	10
00	X_0	X_1	1	
01	X_4	X_5	*	*
11	X_{12}	X_{13}		1
10	X_8	*	X_{11}	*

$K_1 = \bar{M}Q_0 + M\bar{Q}_0$

J_0:

MQ_2 \ Q_1Q_0	00	01	11	10
00	1	X_1	X_3	1
01	1	X_5	X_7	1
11	1	X_{13}	X_{15}	1
10	1	X_9	X_{11}	1

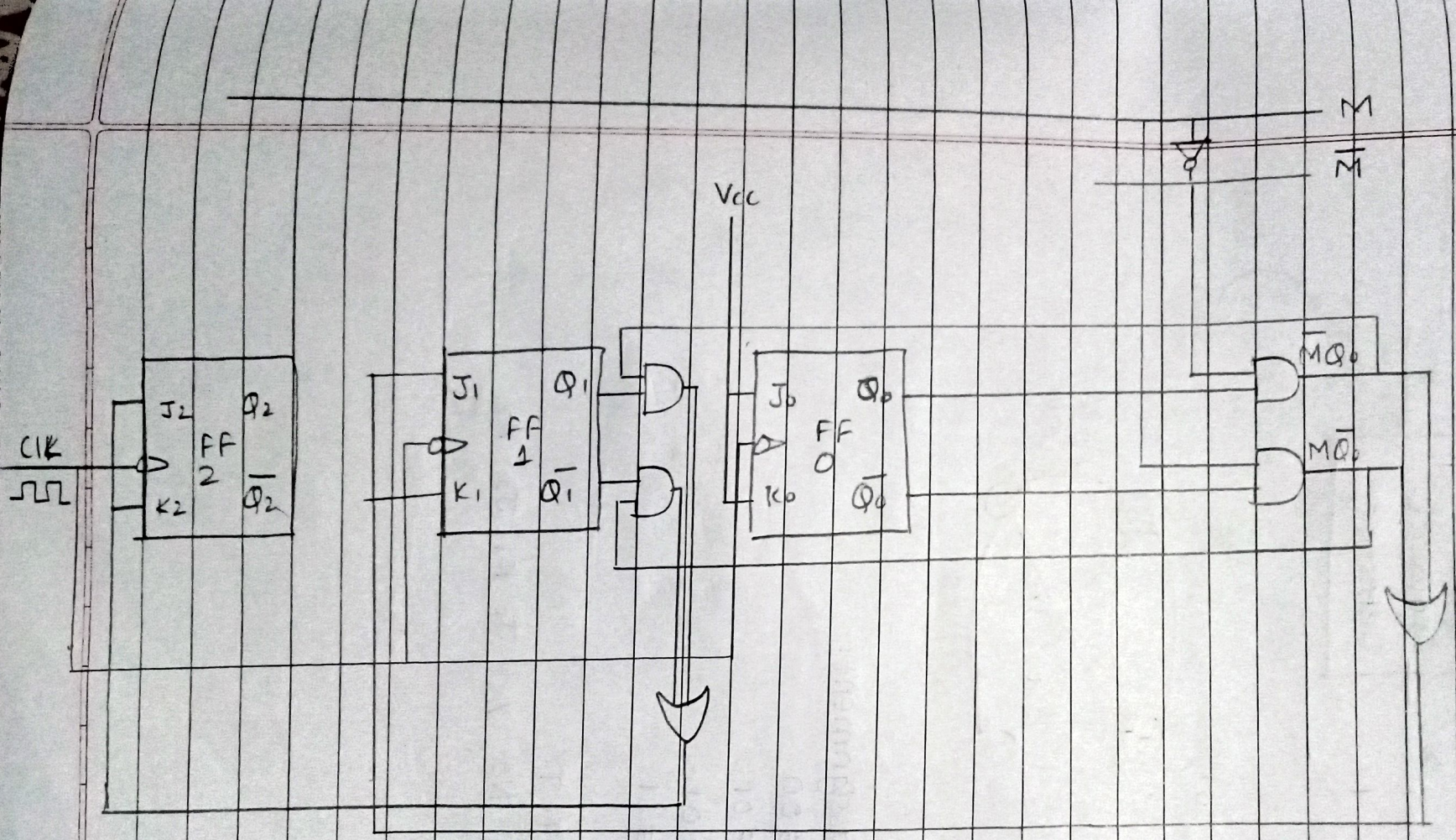
$J_0 = J_0$

K_0:

MQ_2 \ Q_1Q_0	00	01	11	10
00	X_0	1	1	X_2
01	X_4	1	1	X_6
11	X_{12}	1	1	*
10	X_8	1	1	*

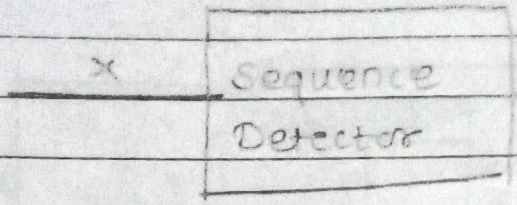
$K_0 = K_0$

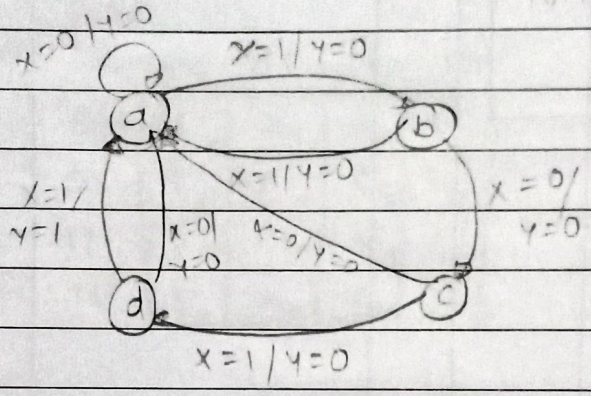
ie. $K_0 = 1$



. All preset and clear are connected to Vcc i.e logic 1.

Q. Design a 1011 sequence detector to detect given sequence using J-K flip flop.





State assignment:

a ≡ 00

b ≡ 01

c ≡ 01

d ≡ 11

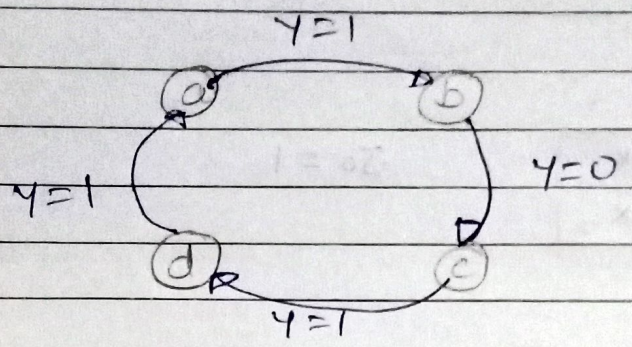
S. T. T.

PS	NS	y	J_1	K_1	J_2	K_2

* Sequence Generator

1011

- State Diagram



State Assignment

$Q_1 Q_0$

a = 00

b = 01

c = 10

d = 11

PS		NS						
Q_1	Q_0	Q_1	Q_0	Y	J_1	K_1	J_0	K_0
0	0	0	1	1	0	X	1	X
0	1	1	0	0	1	X	X	1
1	0	1	1	1	X	0	1	X
1	1	0	0	1	X	1	X	1

- K-map:

J_1 :

Q_1 \ Q_0	0	1
0	0	1
1	X_2	X 3

$\therefore J_1 = Q_0$

K_1:

Q_1 \ Q_0	0	1
0	x	x
1		1

$K_1 = Q_0$

J_0:

Q_1 \ Q_0	0	1
0	1	x
1	1	x

$J_0 = 1$

K_0:

Q_1 \ Q_0	0	1
0	x	1
1	x	1

$K_0 = 1$