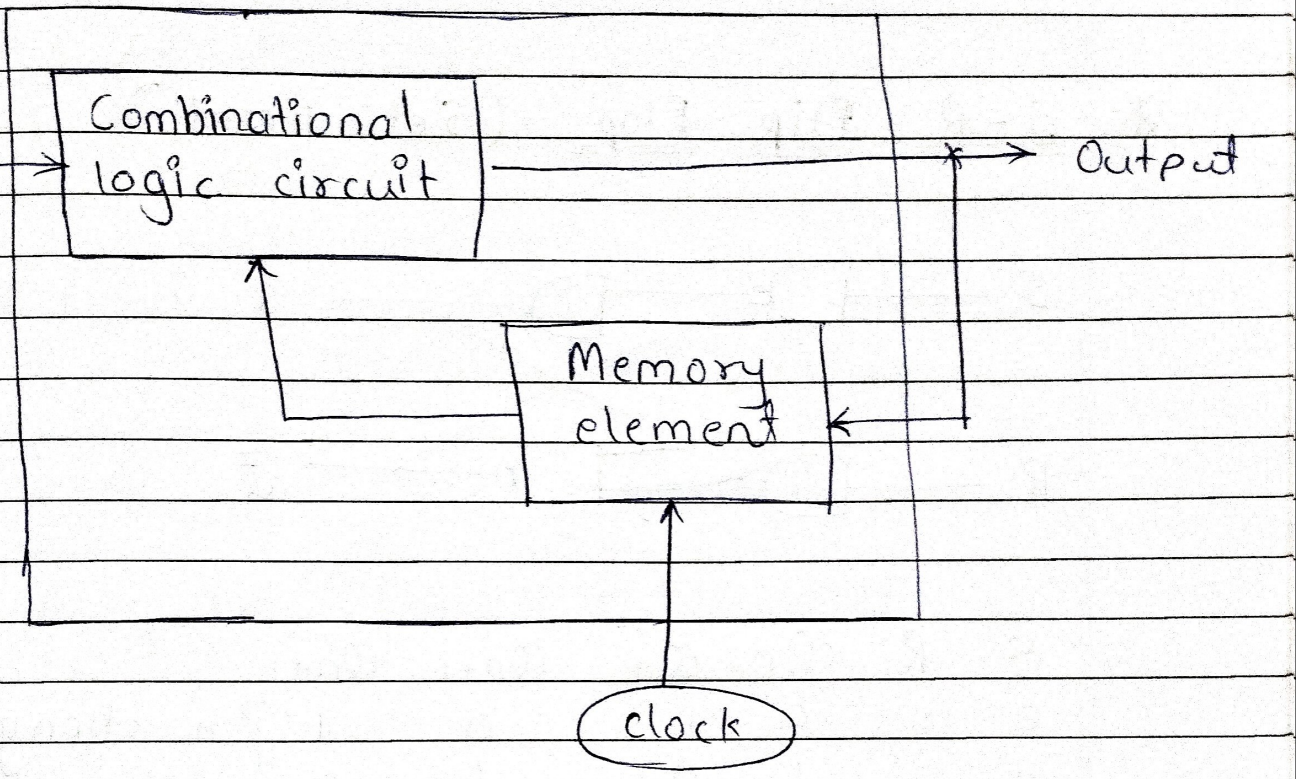
1,1,12B

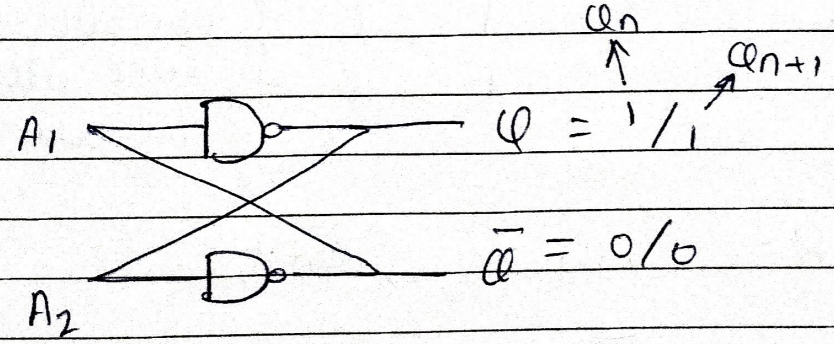
Unit-4

Introduction to Sequential Logic Design

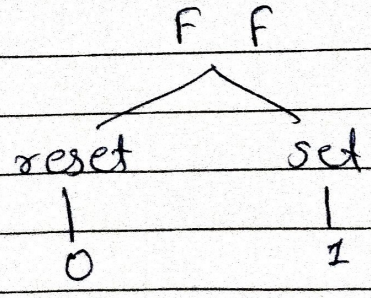


* Sequential Circuits

1 bit memory cell / cross coupled inverter / latch

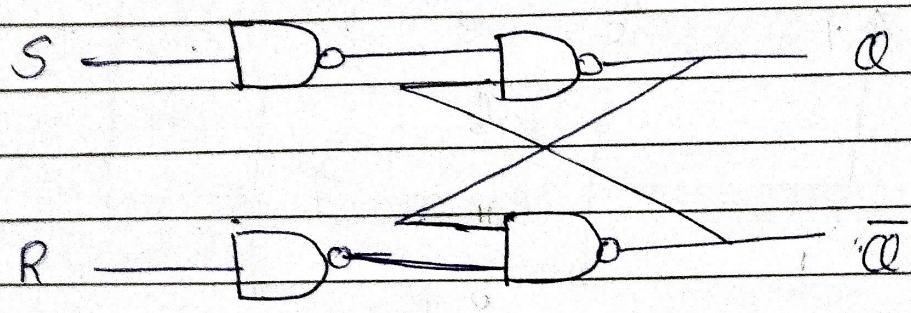


Q_n = Present state
Q_{n+1} = Next-state



Drawback -: No provision to enter the required digital data

* S-R Flip Flop (Set-Reset)



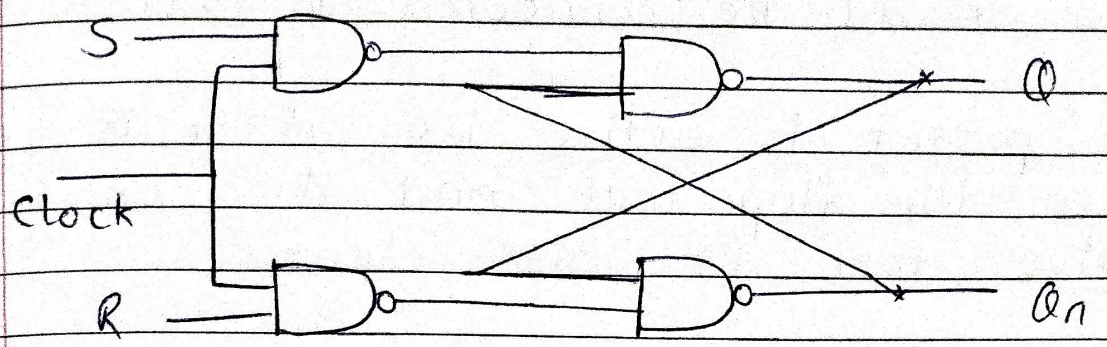
S	R	Q_n	$\bar{Q}_n$	Q_{n+1}	$\bar{Q}_{n+1}$	
0	0	0	1	0	1	} no change
0	0	1	0	1	0	
0	1	0	1	0	1	} Reset
0	1	1	0	0	1	
1	0	0	1	1	0	} set
1	0	1	0	1	0	
1	1	0	1	1	0	} not allowed race around condn
1	1	1	0	1	0	

Case I

(1) $S=0$, $R=0$, $Q_n=0$, $\bar{Q}_n=1$

Q_{n+1} = , $\bar{Q}_{n+1}$ =

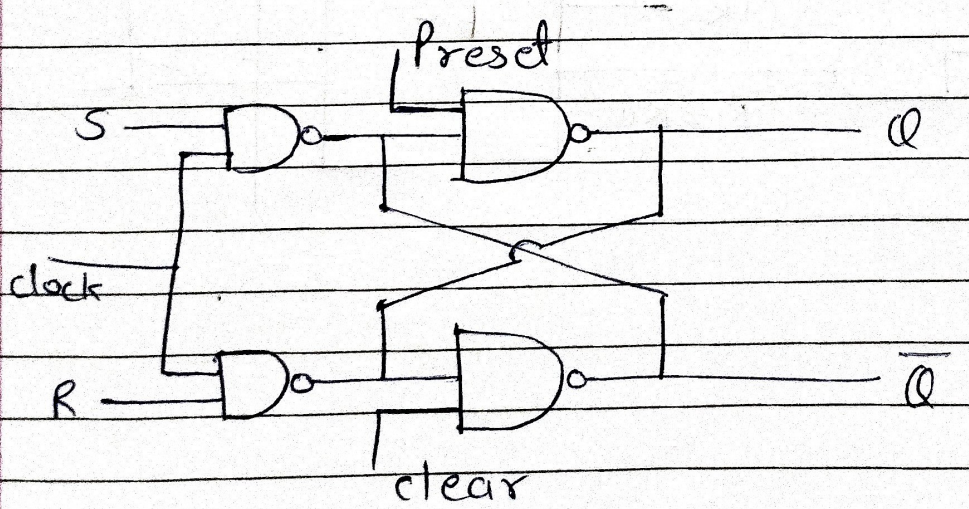
* Clock S-R Flip Flop



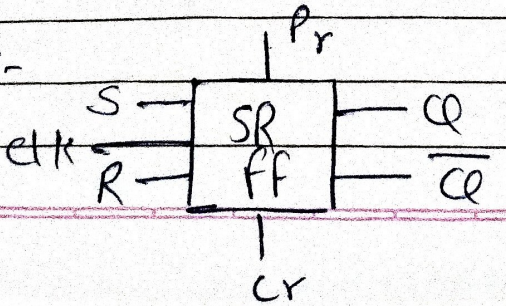
Clock	S	R	Q_{n+1}	$\overline{Q}_{n+1}$
1	0	0	Q_n	$\overline{Q}_n$
1	0	1	0	1
1	1	0	1	0
1	1	1	?	?

* S-R Flip Flop with Preset and Clear

Preset ⟶ resets FF
Clear ⟶ Set FF



Block diagram :-

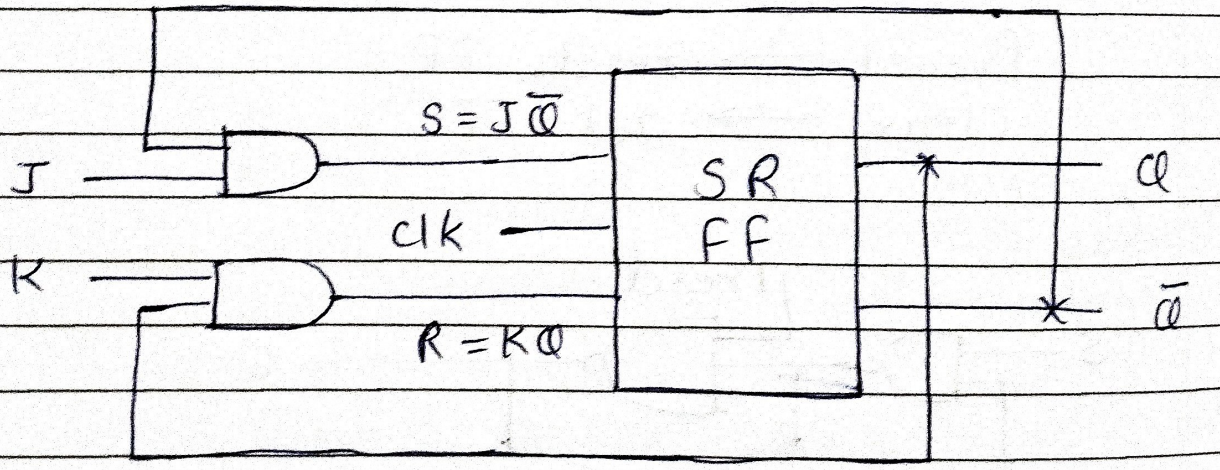


As Preset and Clear are active low for normal working of the flip flop this two should be connected to Vcc

If preset is active i.e if it is zero then flip flop will and if clear is active then FF will clear

Inputs				
Clk	Pr	Cr	O/P	Operation performed
1	1	1	SR FF TT	Normal FF
0	1	0	0	clear
0	0	1	1	set

* JK Flip Flop :-

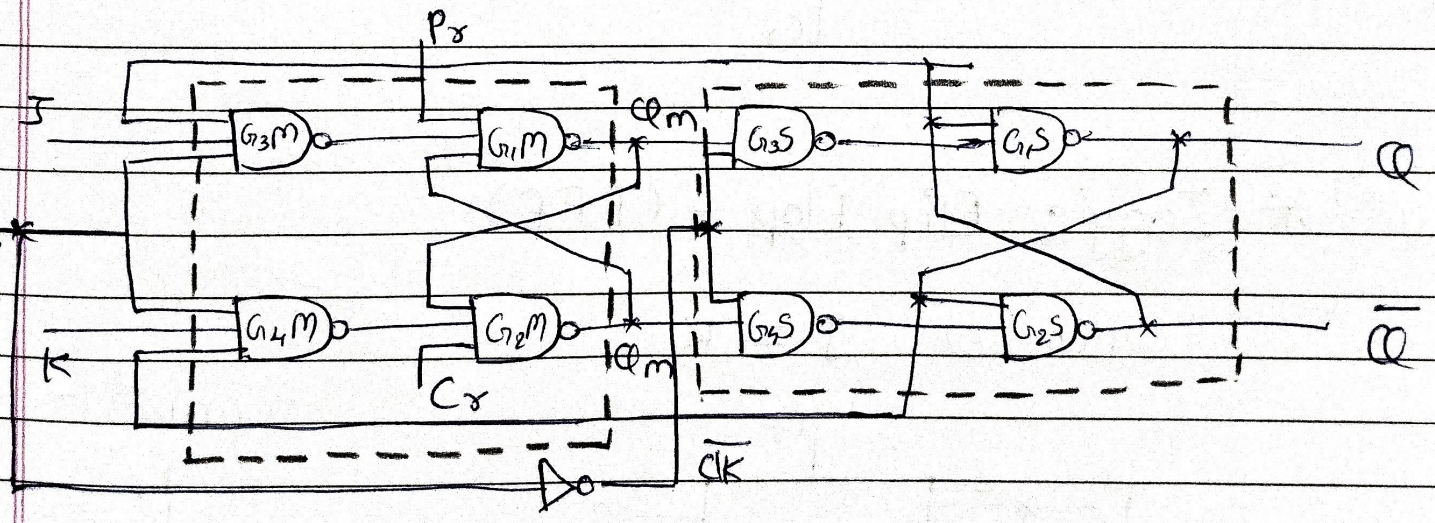


J_n	K_n	Q_n	$\overline{Q}_n$	S_n	R_n	Q_{n+1}	$\overline{Q}_{n+1}$	
0	0	0	1	0	0	0	1	
0	0	1	0	0	0	1	0	
0	1	0	1	0	0	0	1	
0	1	1	0	0	0	0	1	
1	0	0	1	1	0	1	0	
1	0	1	0	0	0	1	0	
1	1	0	1	1	0	1	0	Not allowed
1	1	1	0	0	1	0	1	

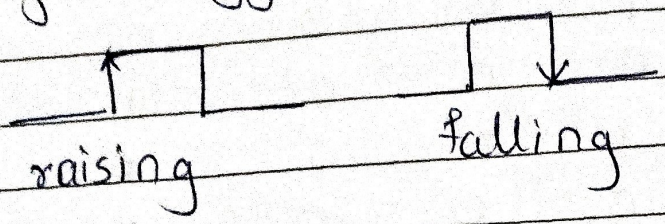
Reduced table

J_n	K_n	Q_{n+1}
0	0	Q_n
0	1	0
1	0	1
1	1	$\overline{Q}_n$

* Master-Slave JK-FF

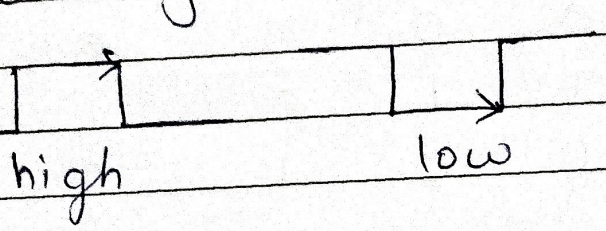


Edge triggered



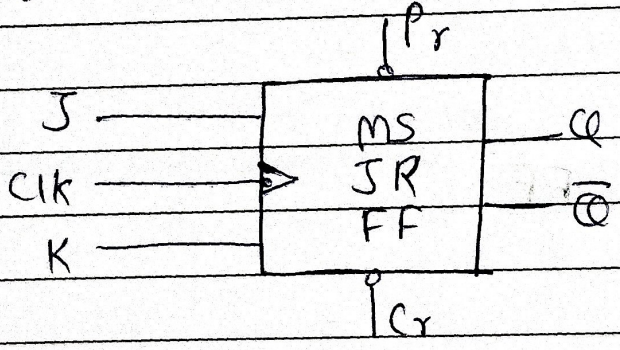
they are +ve &

Level triggered



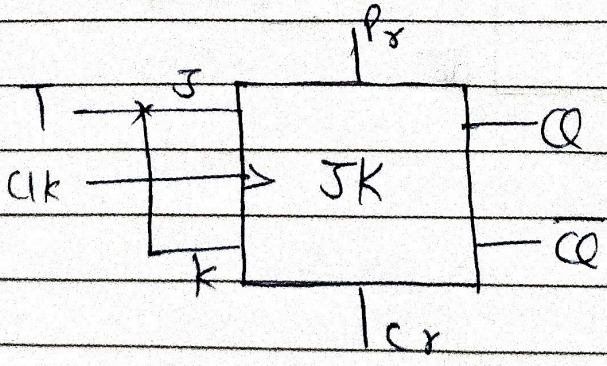
Circuit changes its state at high level and low level that is level.

- Symbol of Master Stake JK-FF

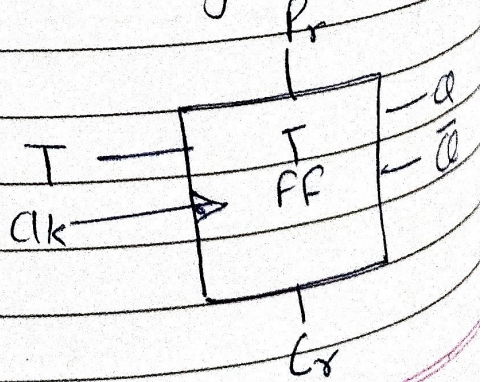


(M) * Toggle Flip Flop - (TFF)

whenever J = K



Symbol:-



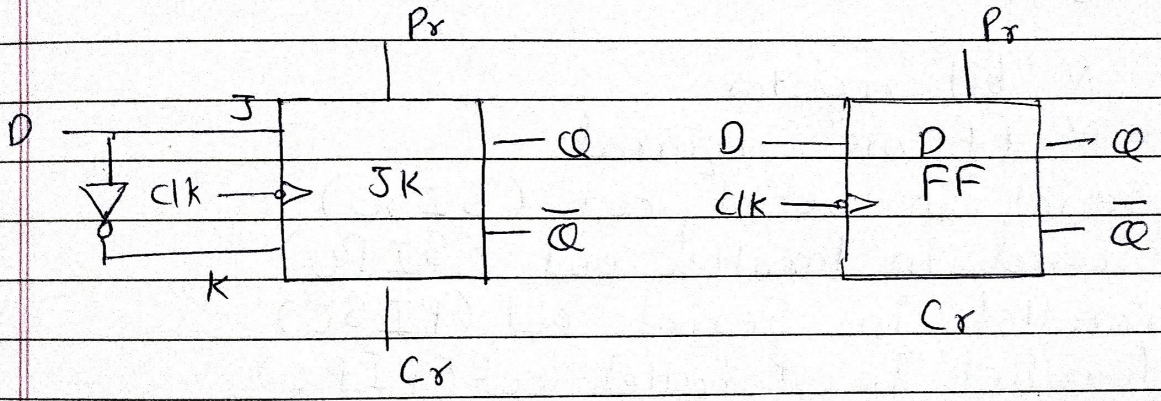
Truth Table –

IC – 7476

Input	Output
T_n	Q_{n+1}
0	Q_n
1	$\overline{Q_n}$

If T = 1, T FF acts as Toggle switch i.e for every clock pulse output changes.

* **DFF – Delay Flip Flop**



In Delay FF the input data appears at the output at the end of the clock pulse i.e. the transfer of data from i/p to o/p is delayed and, hence the name is DFF.

I/P	O/P
D_n	Q_{n+1}
0	0
1	1

Imp

* Excitation table of Flip Flops

Present state	Next state	SRFF		JKFF		TFF	DFF
Q_n	Q_{n+1}	S_n	R_n	J_n	K_n	T_n	D_n
0	0	0	X	0	X	0	0
0	1	1	0	1	X	1	1
1	0	0	1	X	1	1	0
1	1	X	0	X	0	0	1

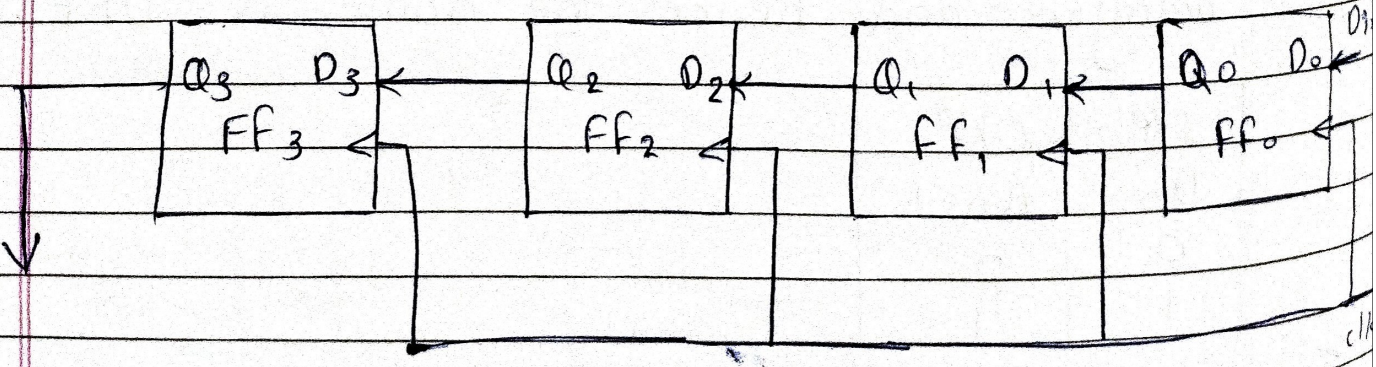
* Application of flip flop

1) Registors - collection of flip flops

N bit register
N FF are required.

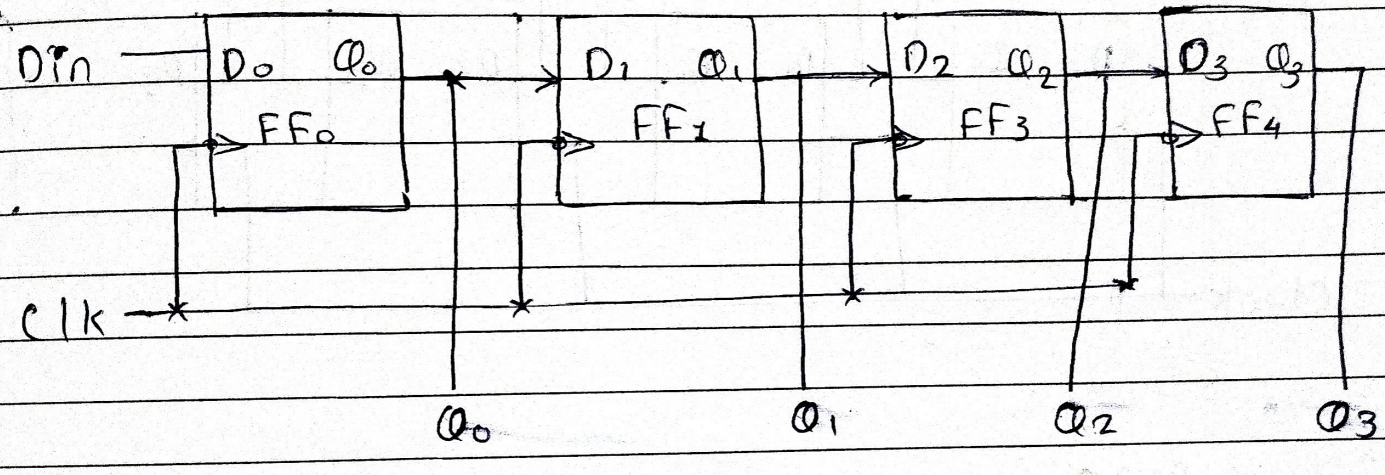
1) Serial in Serial out (SISO)
2) Serial in Parallel out (SIPO)
3) Parallel in Serial out (PISO)
4) Parallel in Parallel out (PIPO)

* Serial in Serial out → left shift



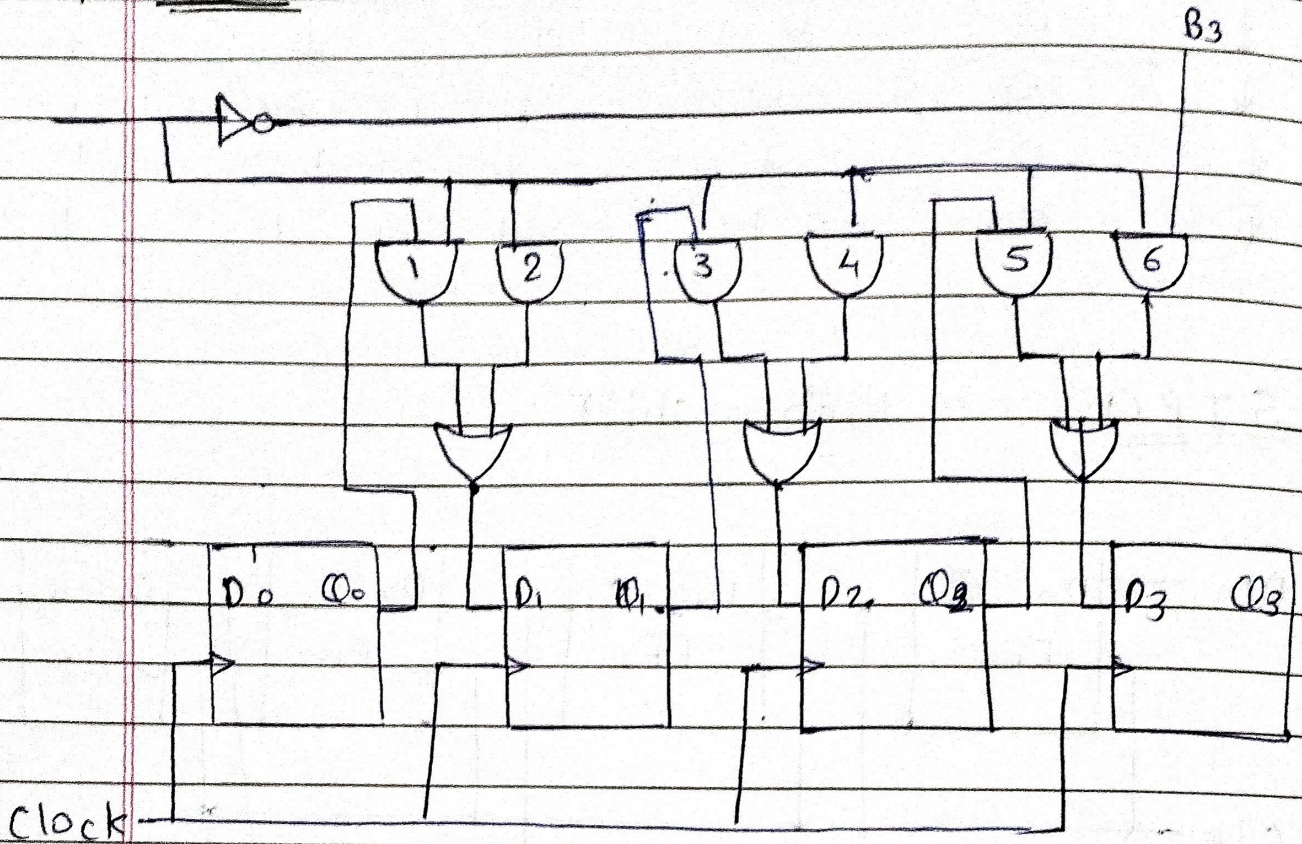
Clk	$Q_3 = D_3$	$Q_2 = D_2$	$Q_1 = D_1$	$Q_0 = D_0$	Din
↓	0	0	0	1	1
↓	0	0	1	1	1
↓	0	1	1	1	1
↓	1	1	1	1	1

* **SIPO** → Right shift



Here, data is loaded bit by bit first till the time outputs are disabled. As soon as loading is completed and all the flip flop contains the required data the outputs are enabled so that loaded data is made available over the all output lines simultaneously

* PISO

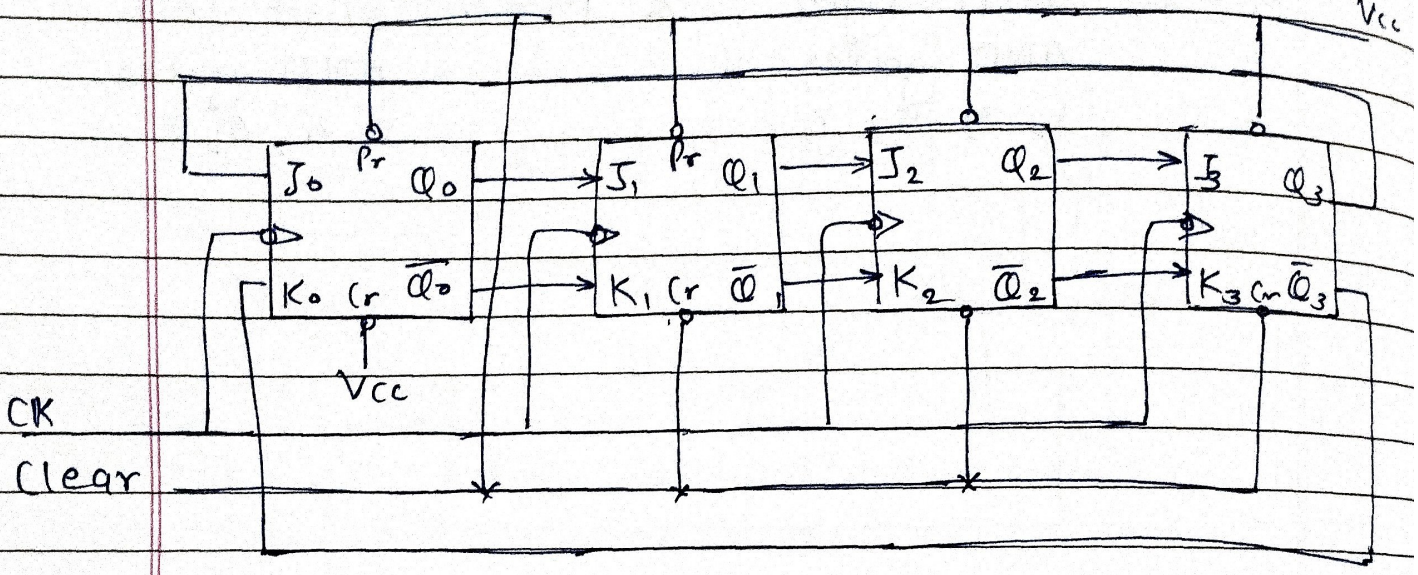


* PIPO

IMP

* 4 bit Ring Counter

Q1 Draw and explain 4 bit Ring Counter
Q2 with diagram explain working of -

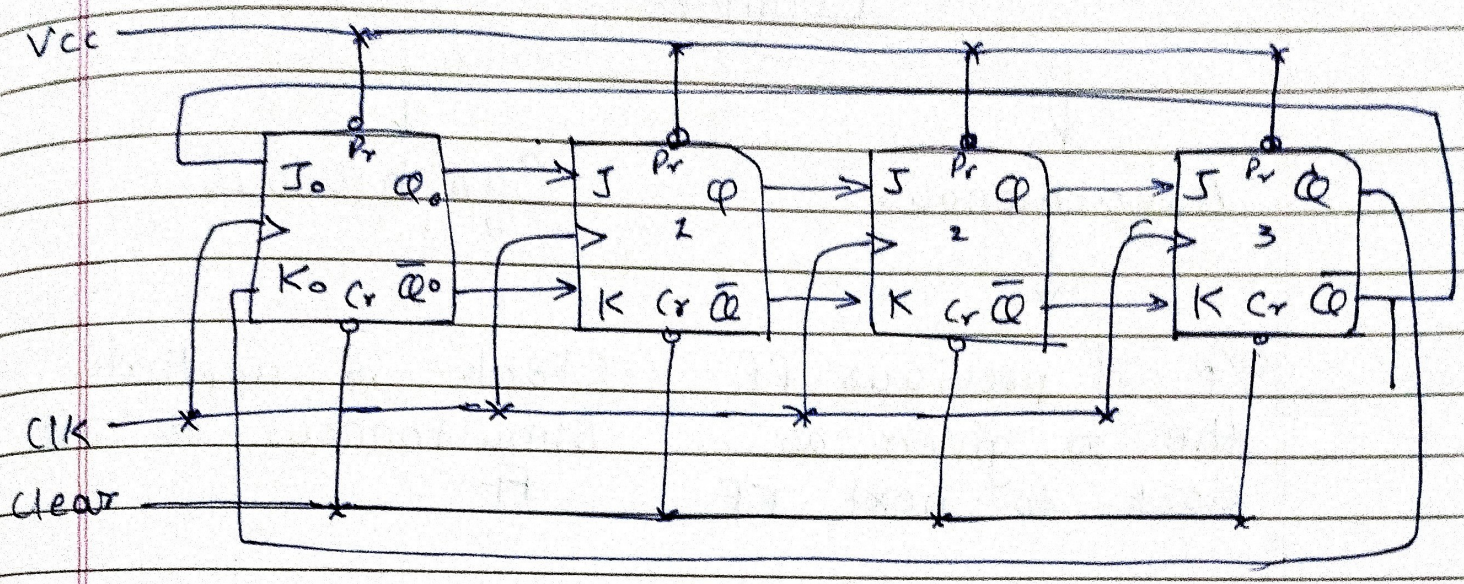


Clk	Q_0	Q_1	Q_2	Q_3
X				
↓	1	0	0	0
↓	0	1	0	0
↓	0	0	1	0
↓	0	0	0	1

1 Pulse is being circulated

IMP

* 4 bit Twisted Ring Counter / Johnson's Counter / Moebius



Clk	Q_0	Q_1	Q_2	Q_3
↓	0	0	0	0
↓	1	0	0	0
↓	1	1	0	0
↓	1	1	1	0
↓	1	1	1	1
↓	0	1	1	1
↓	0	0	1	1
↓	0	0	0	1